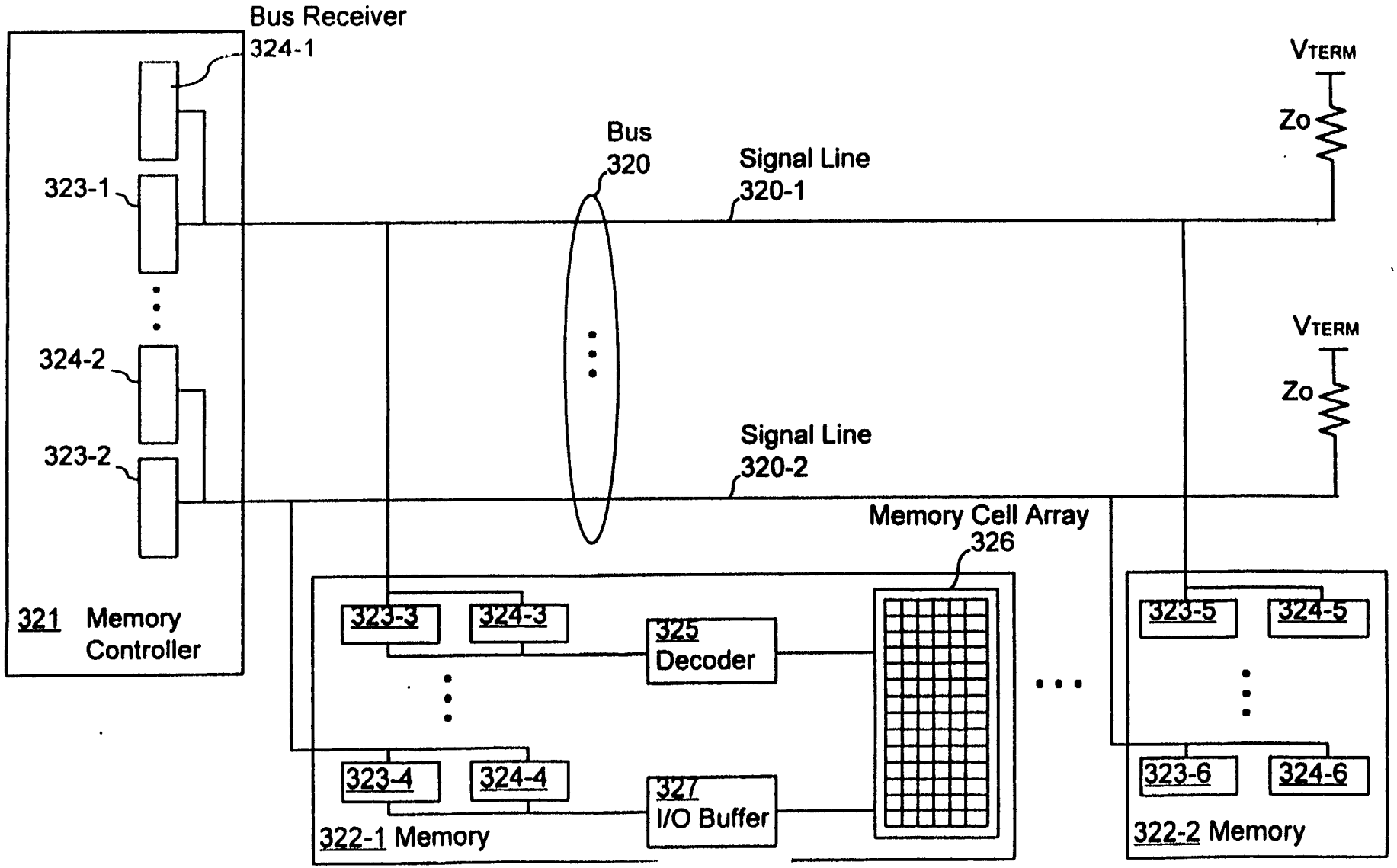

Bus Receiver
324-1
323-1
324-2
323-2
321 Memory Controller
Bus
320
Signal Line
320-1
Signal Line
320-2
VTERM
Zo
VTERM
Zo
Memory Cell Array
326
323-3
324-3
325
Decoder
323-4
324-4
327
I/O Buffer
322-1 Memory
323-5
324-5
323-6
324-6
322-2 Memory

FIG. 1

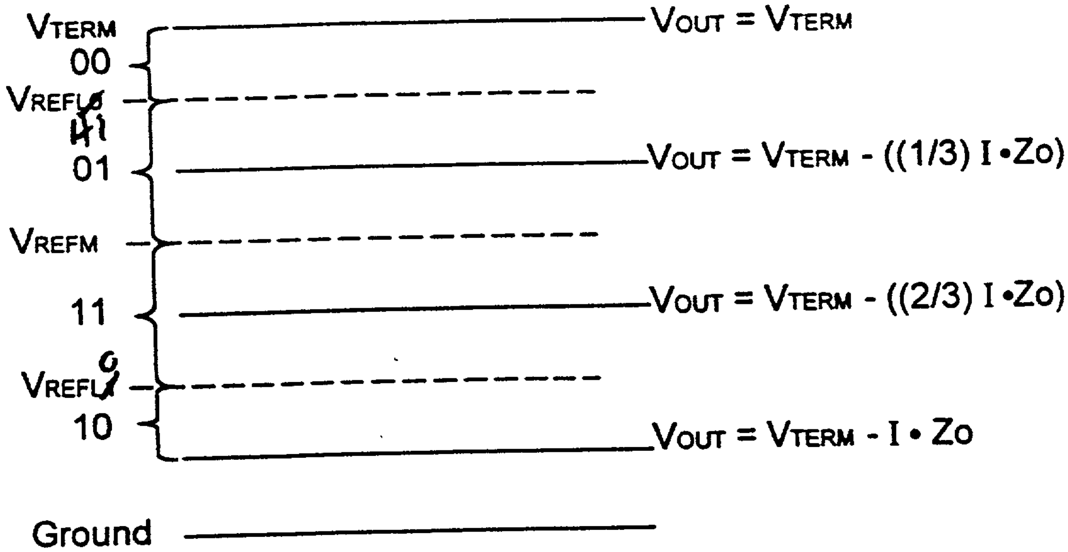


FIG. 2

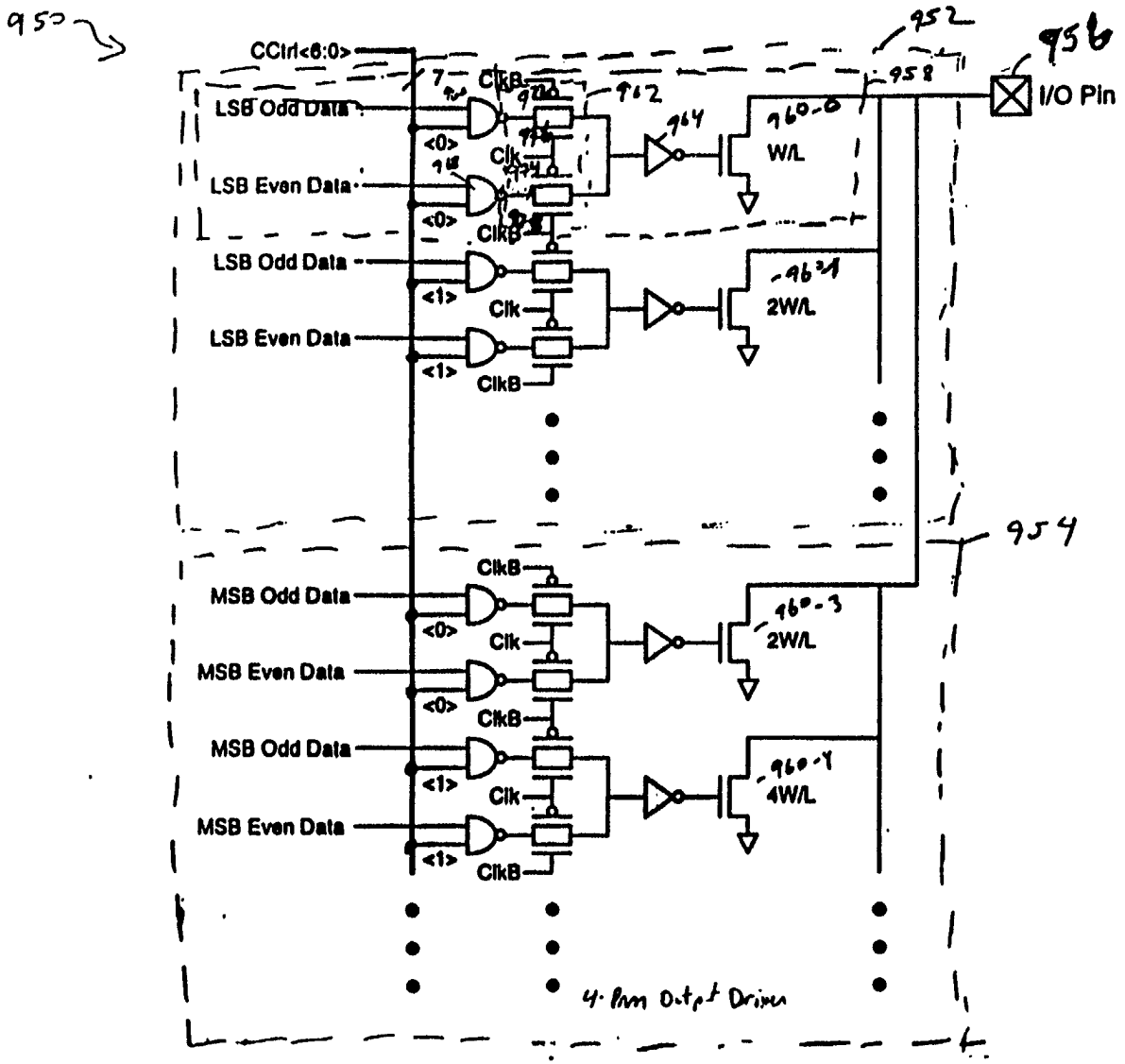

950
952
956
958
I/O Pin
CCtrl<6:0>
LSB Odd Data
LSB Even Data
MSB Odd Data
MSB Even Data
<0>
<1>
Clk
ClkB
962
964
960-0
W/L
960-1
2W/L
960-3
2W/L
960-4
4W/L
954
4-Pin Output Driver

FIG. 3A

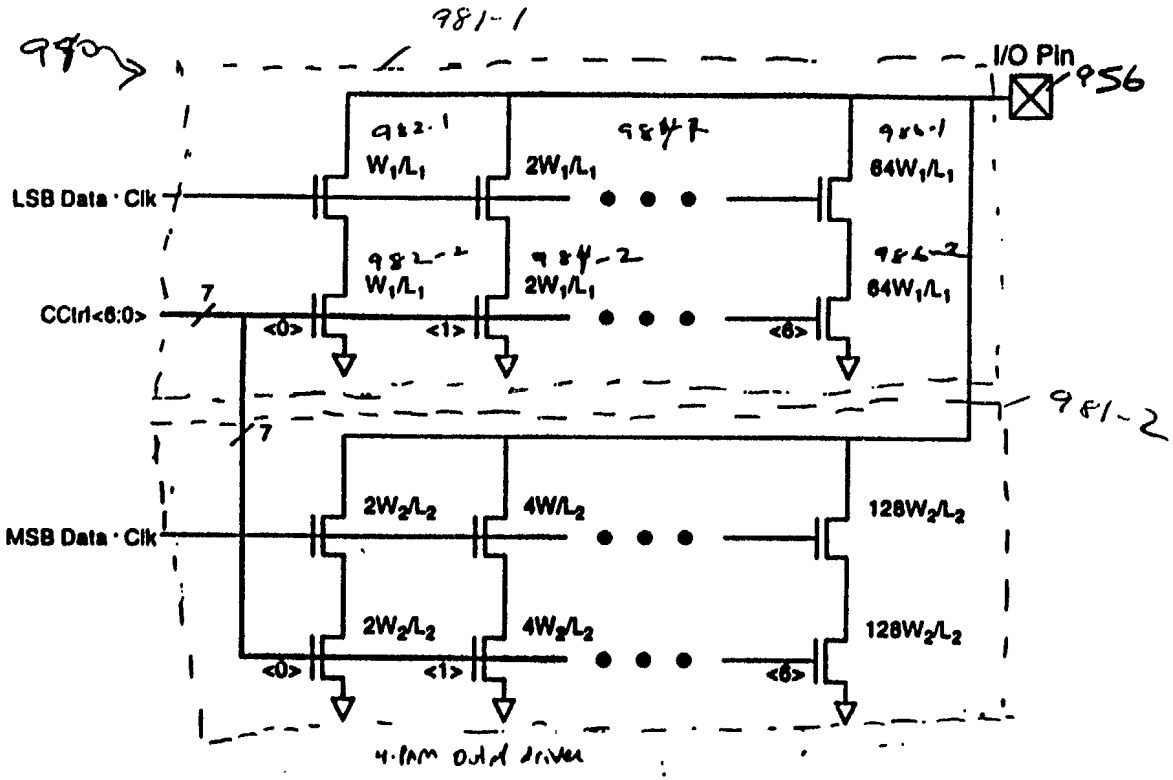


FIG 3B

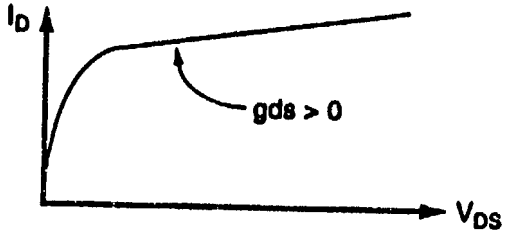


FIG 4A

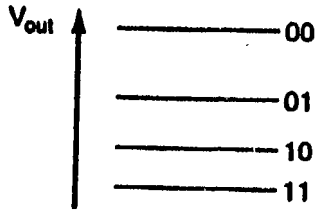


FIG. 4B

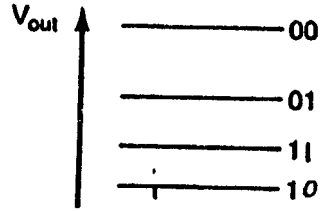
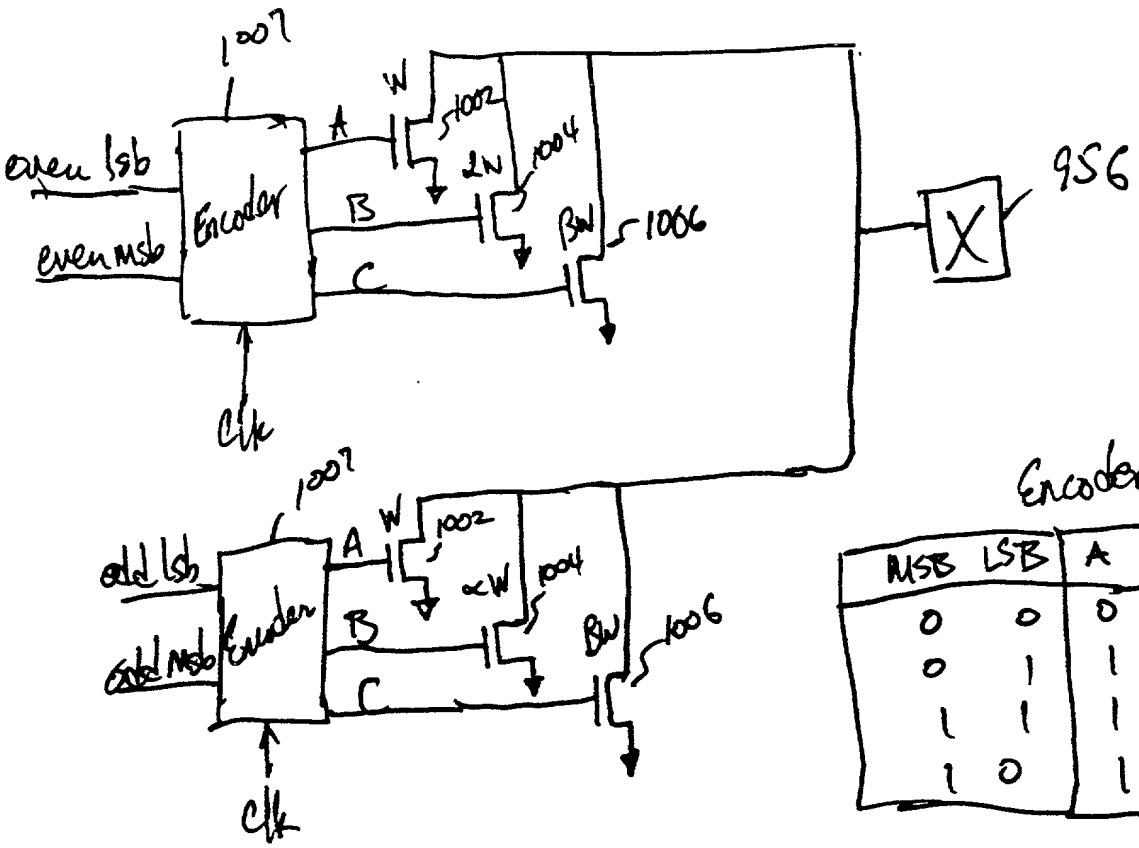


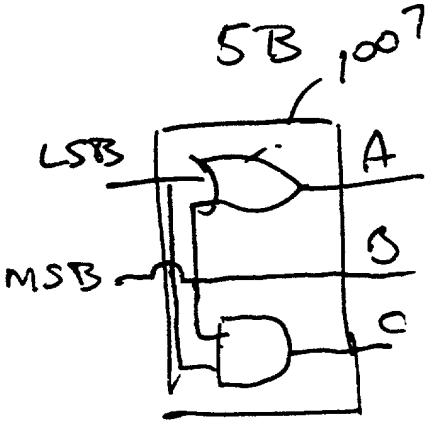
FIG. 4C

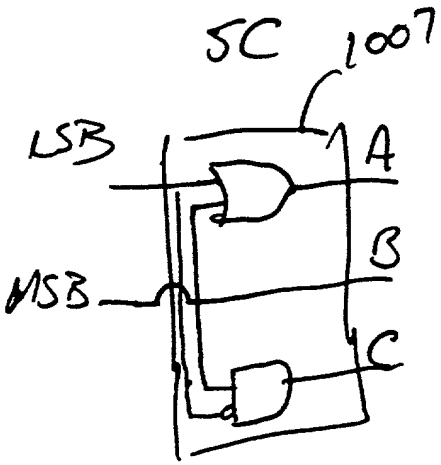
FIG. 5A

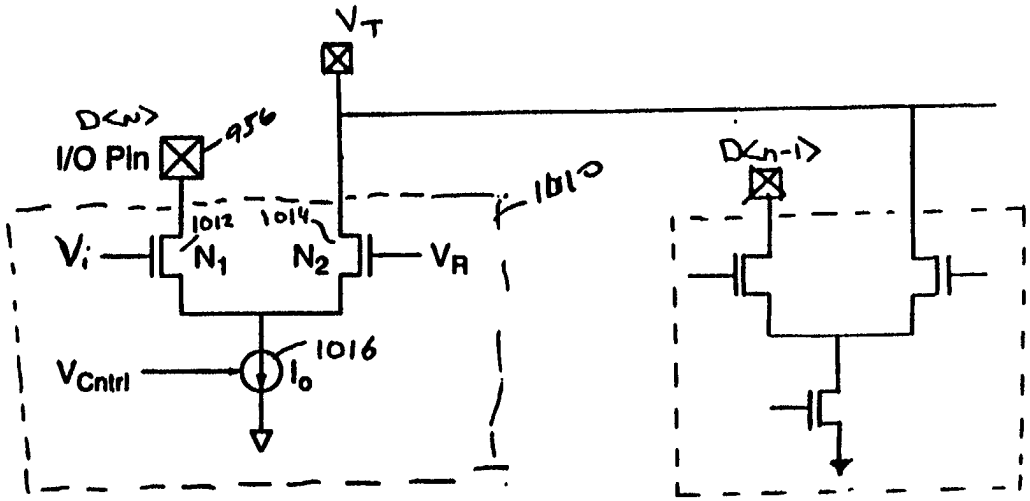


Encoder logic

MSB	LSB	A	B	C
0	0	0	0	0
0	1	1	0	0
1	1	1	1	0
1	0	1	1	1







circuit to Reduce Switching Noise

FIG 6

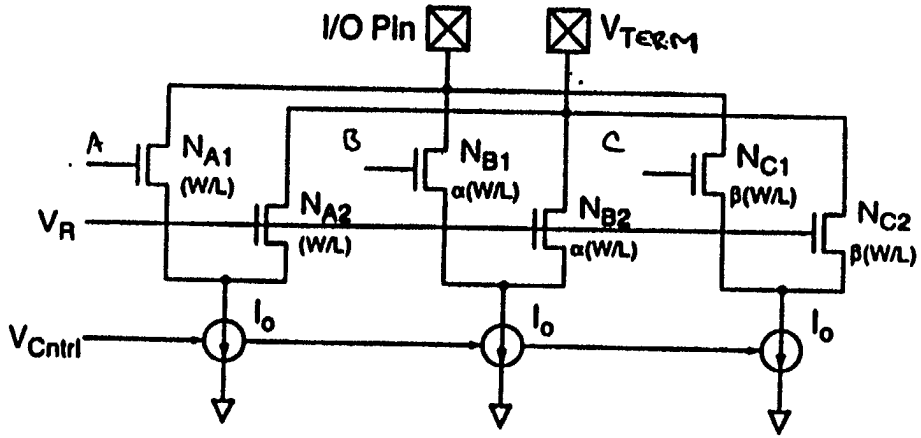
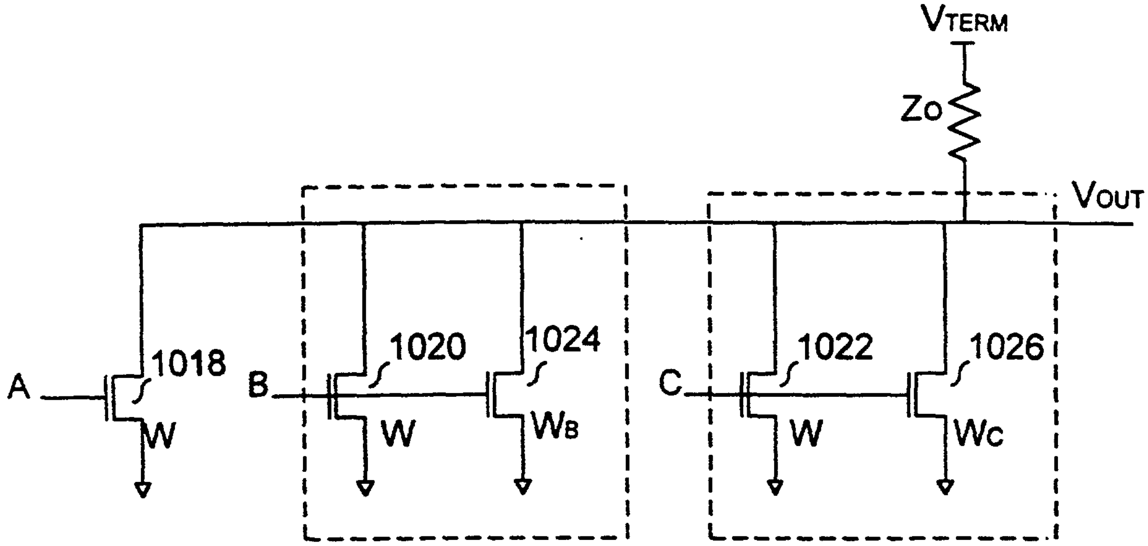
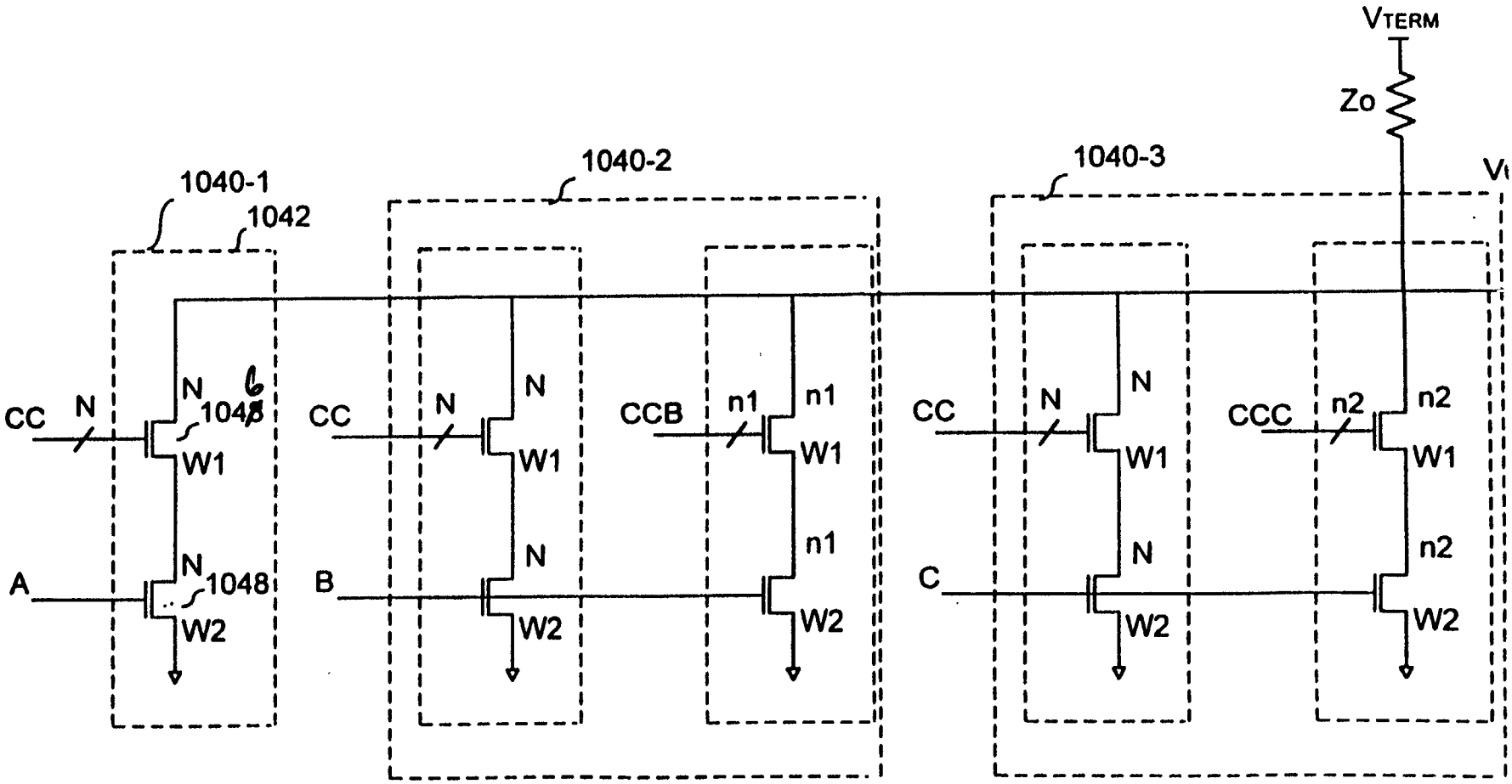


FIG. 7



GDS Compensated Multi-PAM Output Driver

FIG. 8



GDS Compensated Multi-PAM Output Driver with Current Control

FIG. 9A

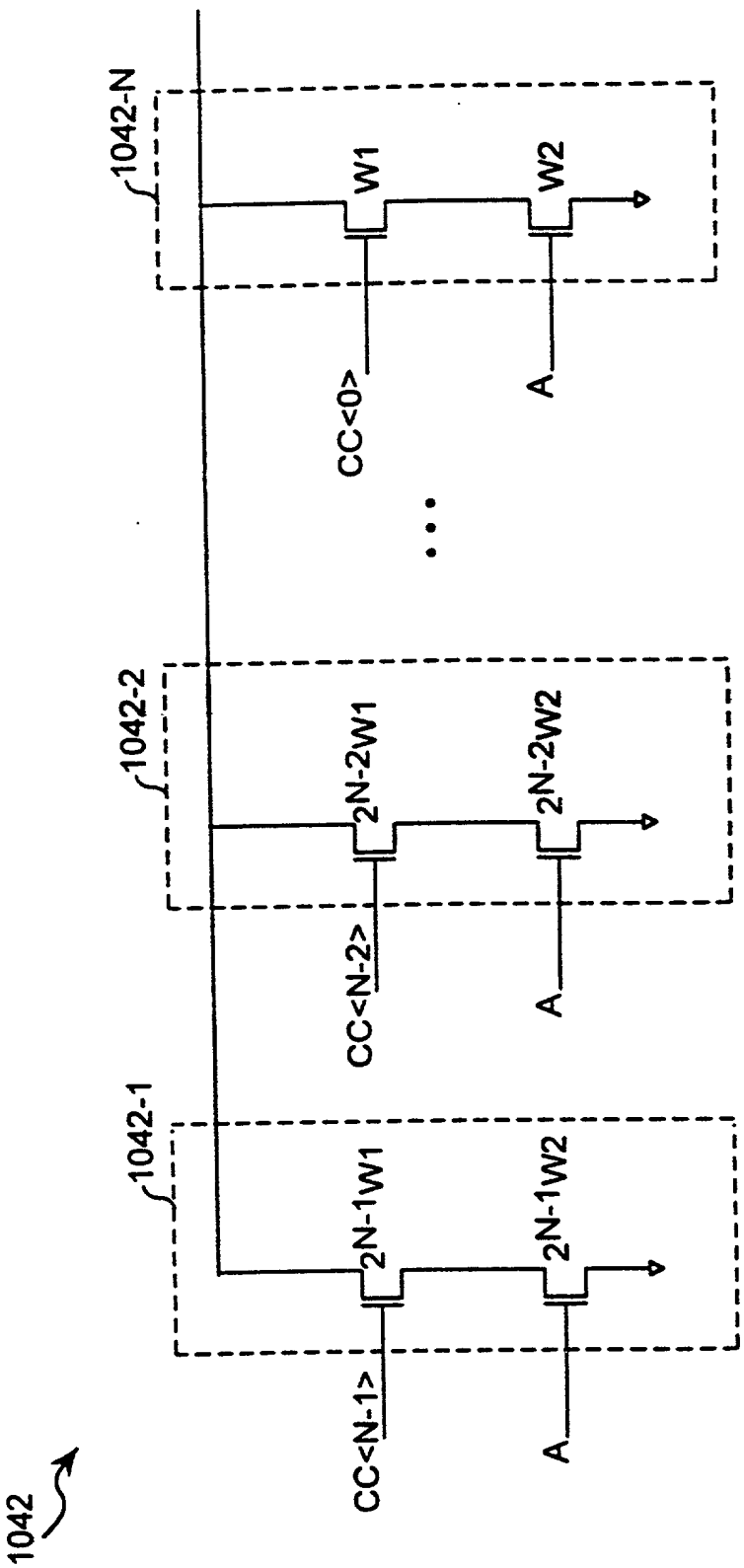

1042
1042-1
1042-2
1042-N
2N-1W1
2N-1W2
2N-2W1
2N-2W2
W1
W2
CC<N-1>
CC<N-2>
CC<0>
A
A
A

FIG. 9B

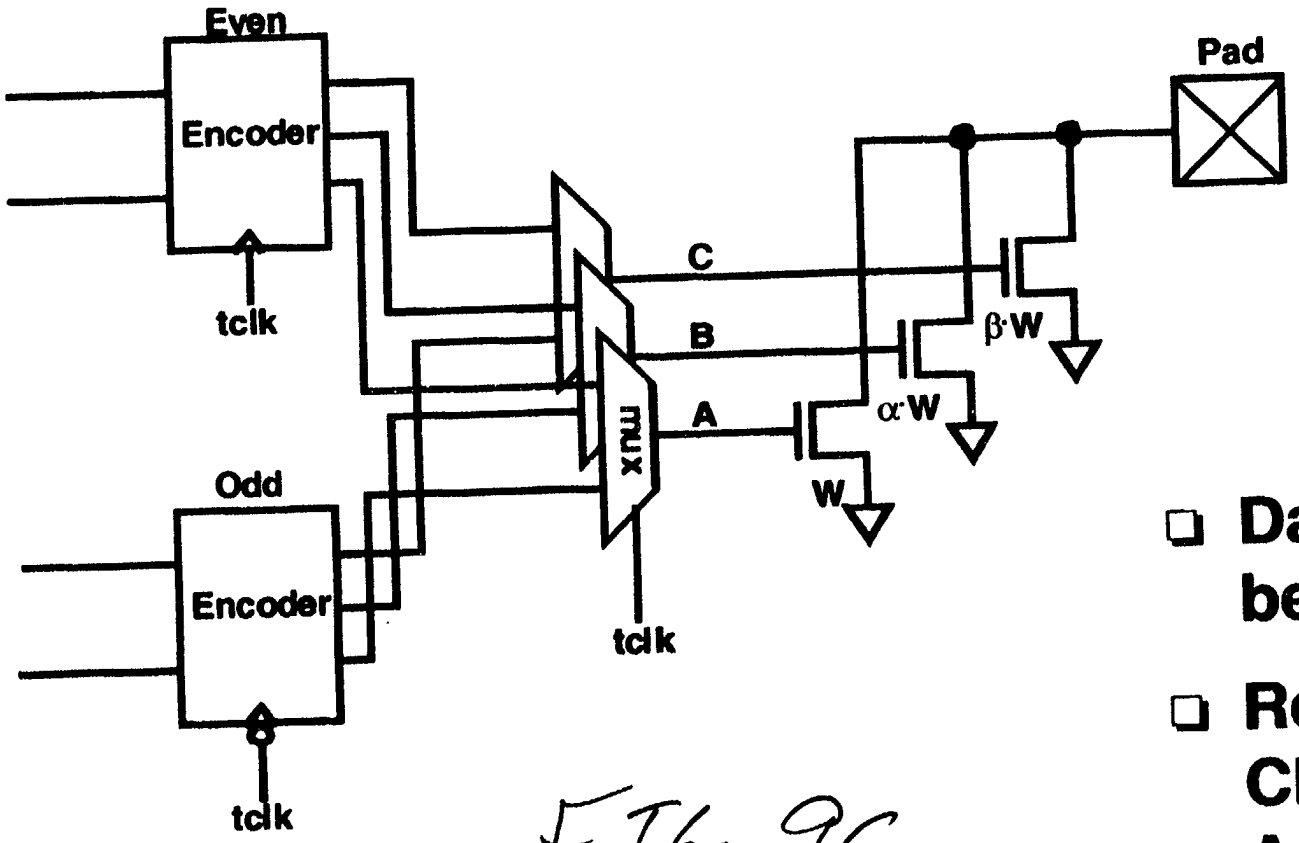
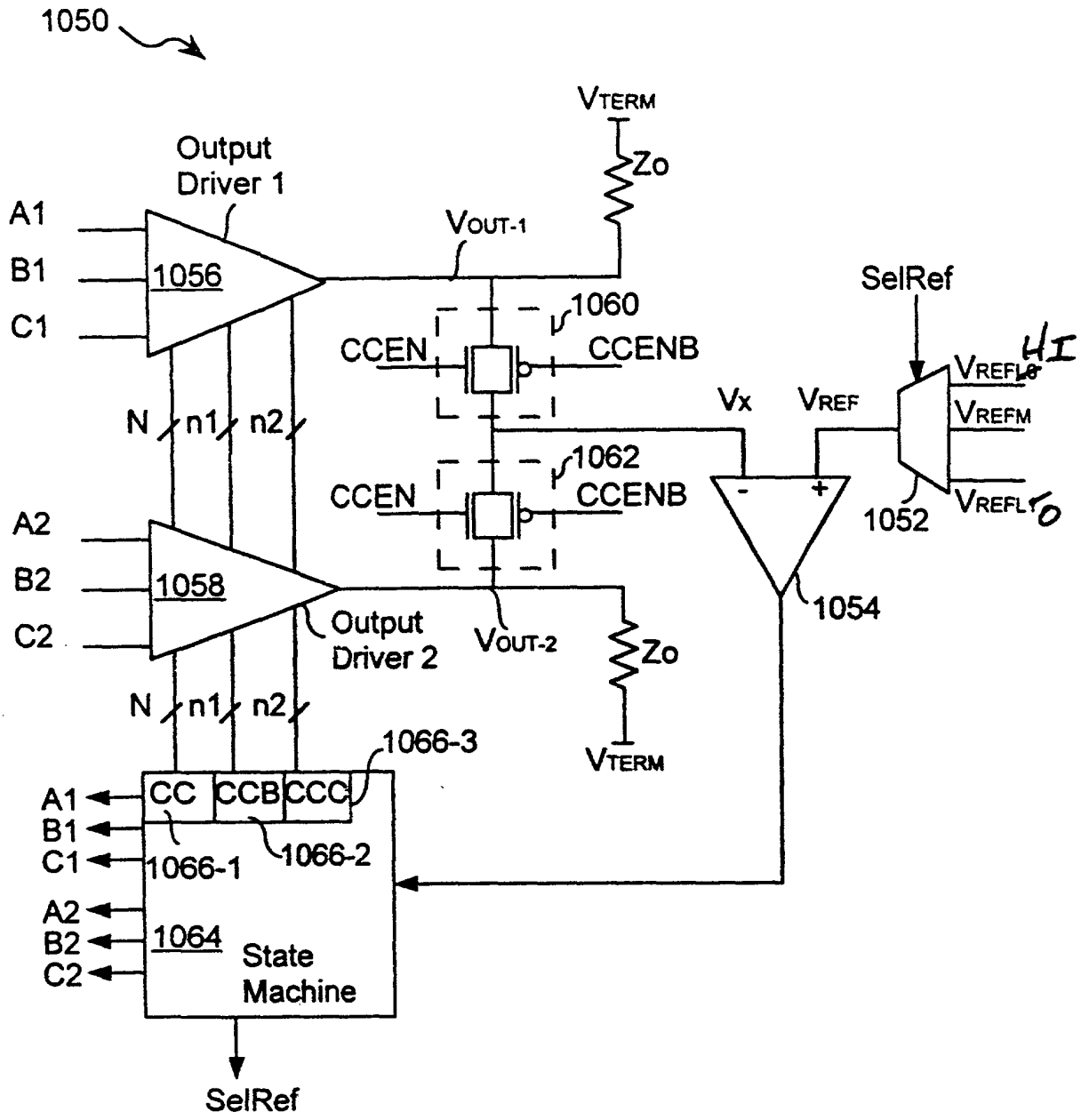


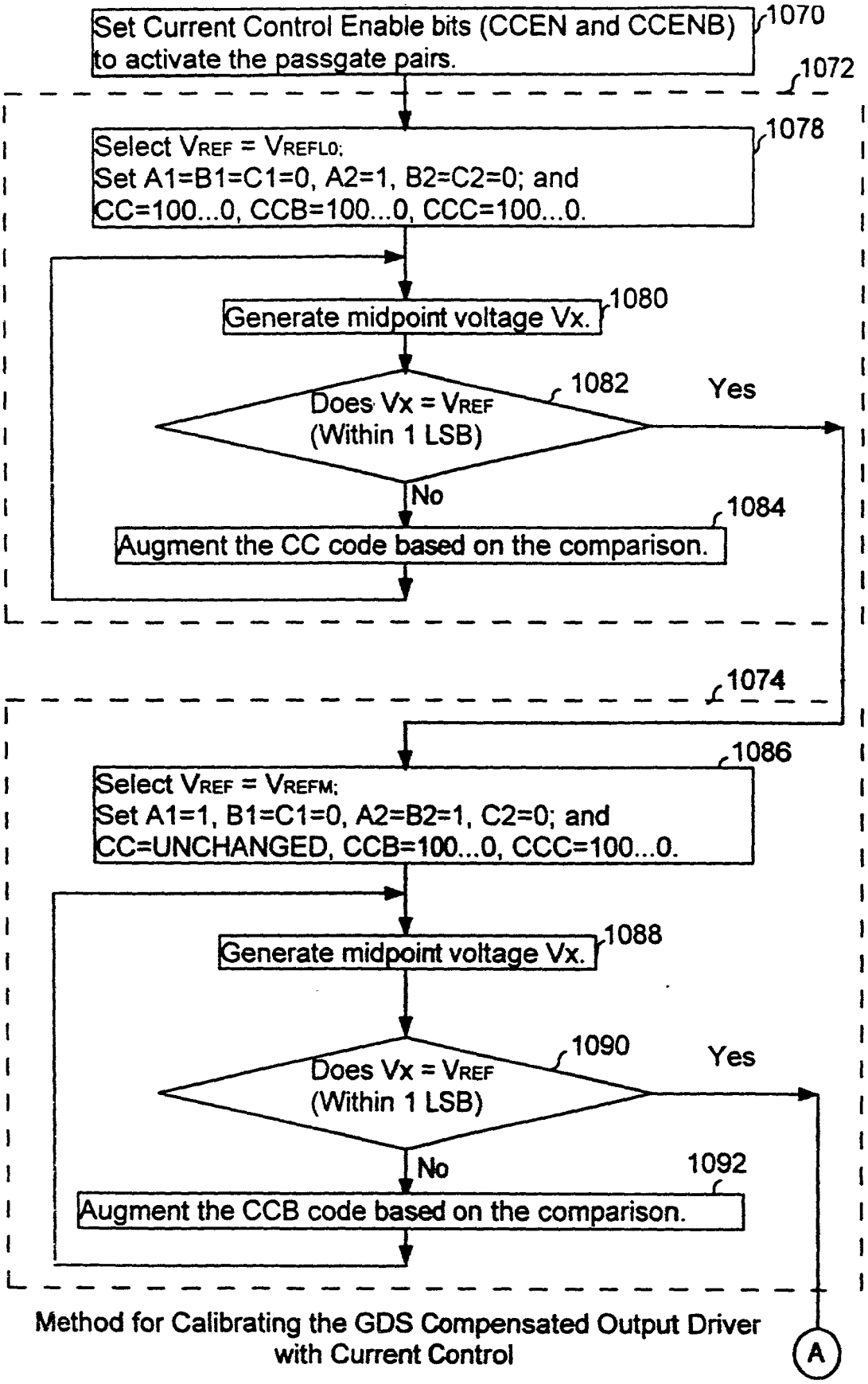
FIG. 9C

- Data muxed before pad
- Requires running CMOS signals A,B,C @ full frequency



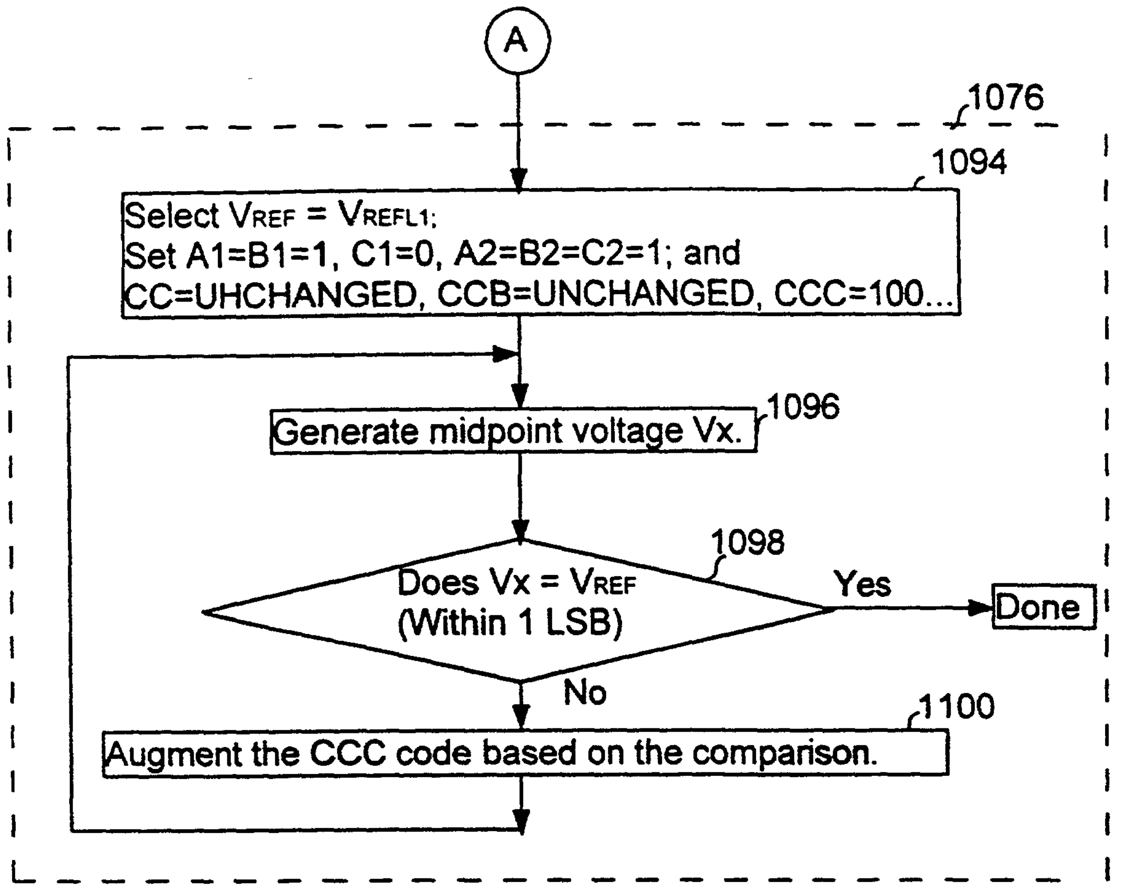
Circuit for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 10



Method for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 11A



Method for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 11B

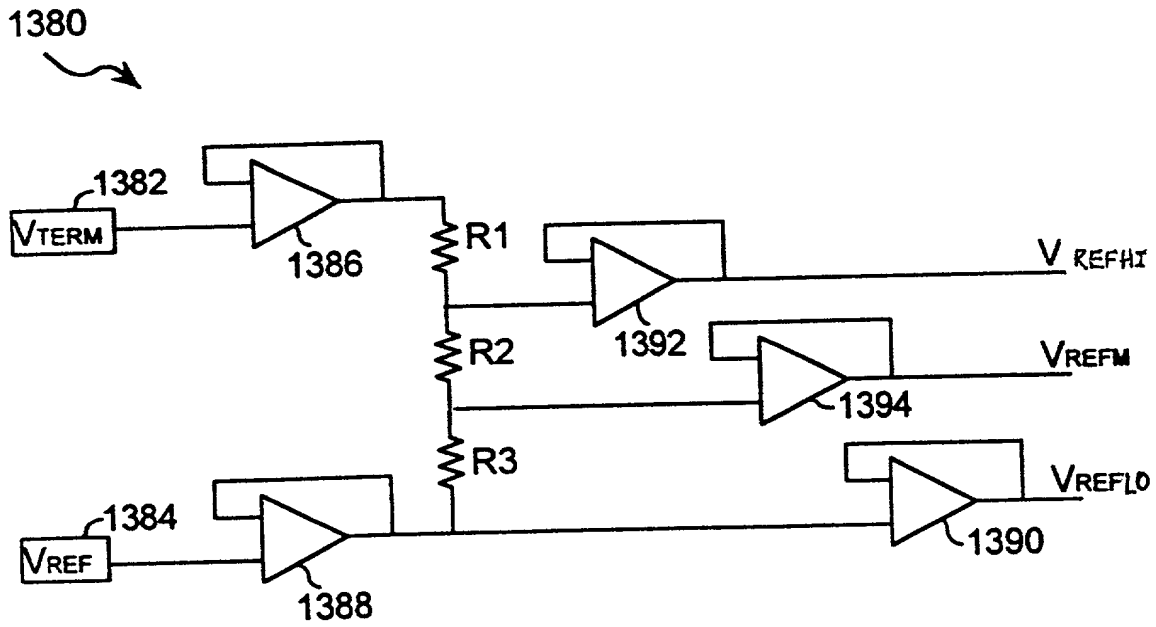


FIG. 12

FIG 13A

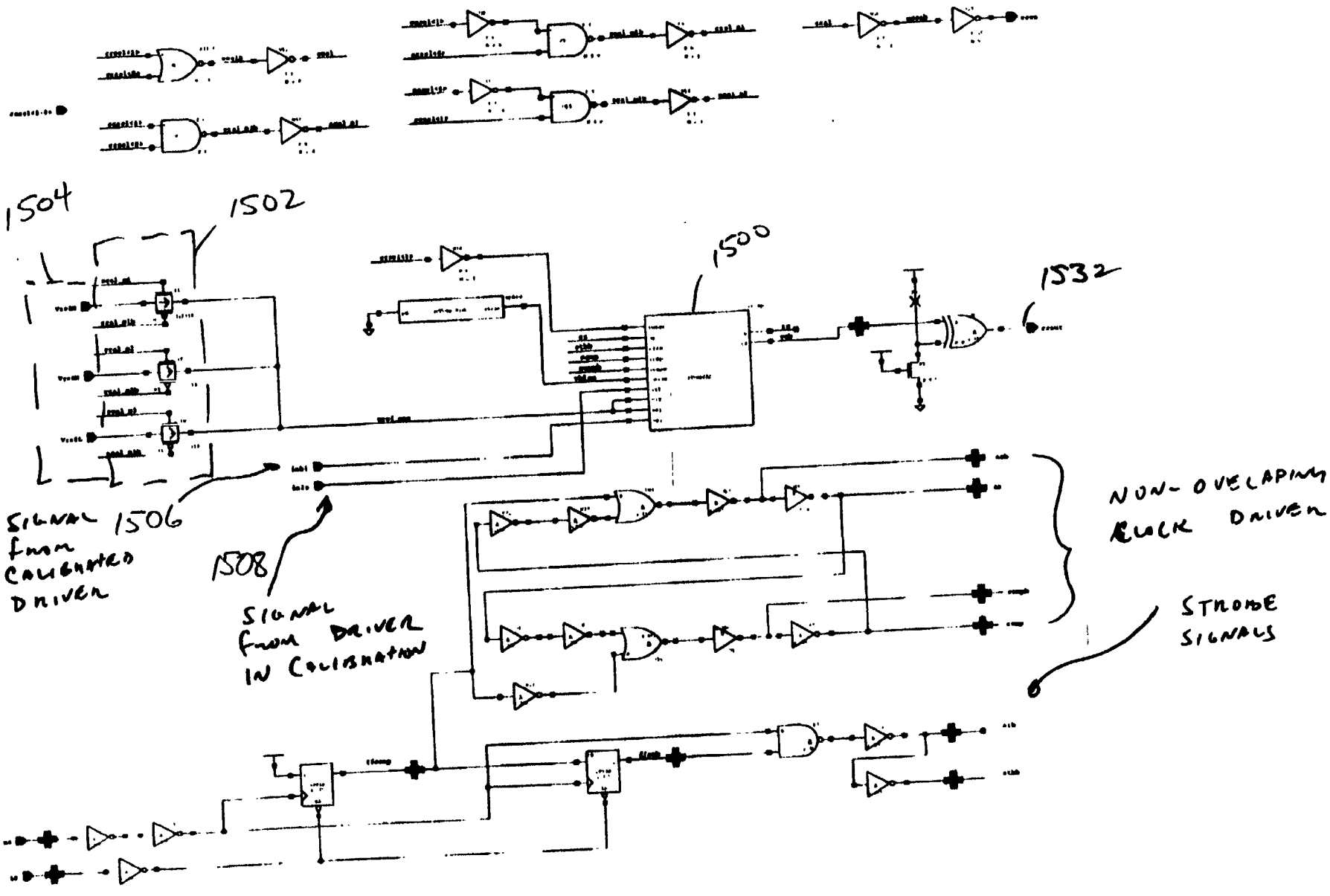
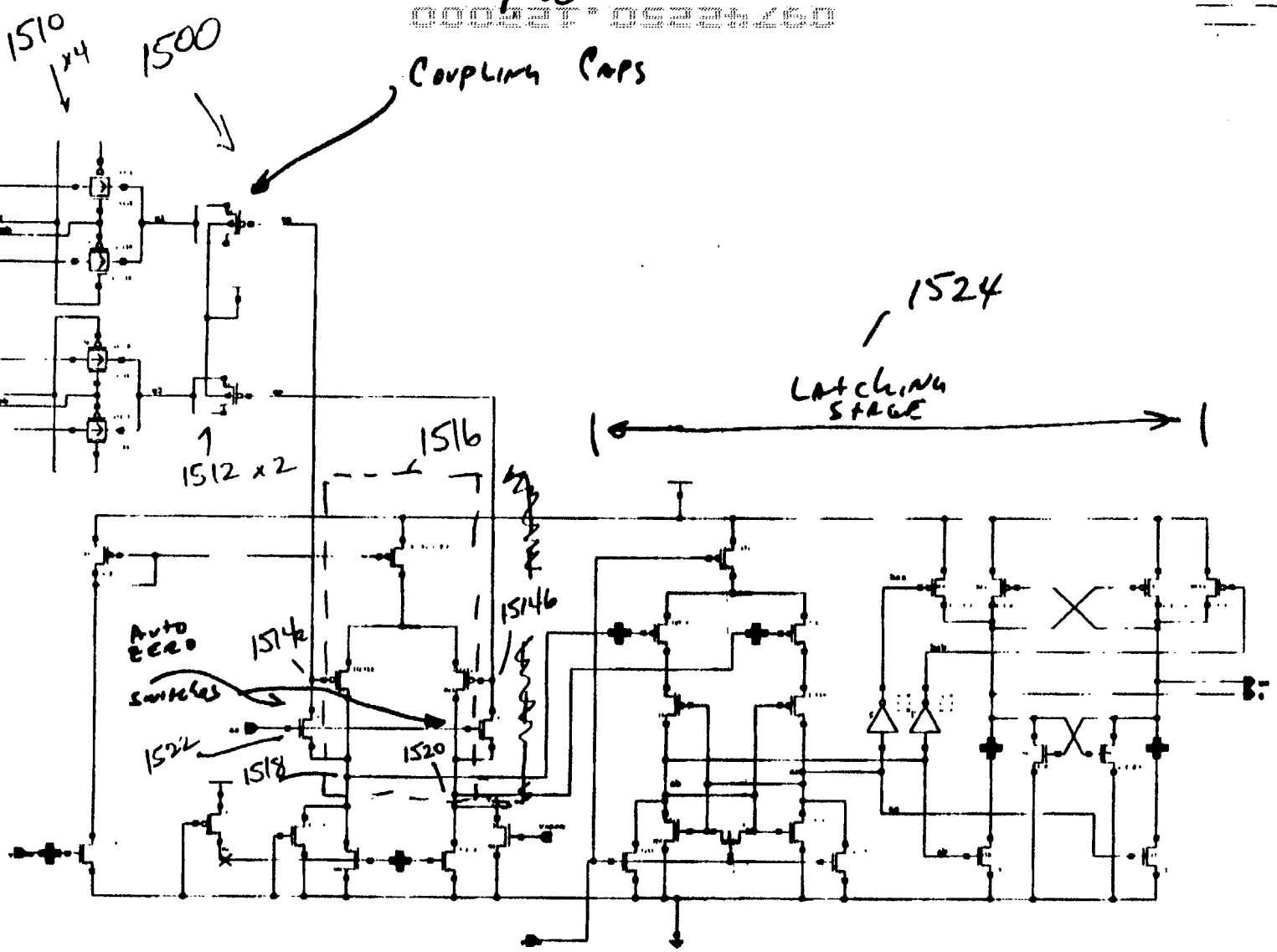

1504
1502
1500
1532
SIGNAL 1506 FROM CALIBRATED DRIVER
1508
SIGNAL FROM DRIVER IN CALIBRATION
NON-OVERLAPING CLOCK DRIVER
STROBE SIGNALS

Fig 13B


1510
x4
1500
Coupling Caps
1524
Latching Stage
1516
1512 x2
1514b
1514a
Auto Ecal switches
1522
1518
1520

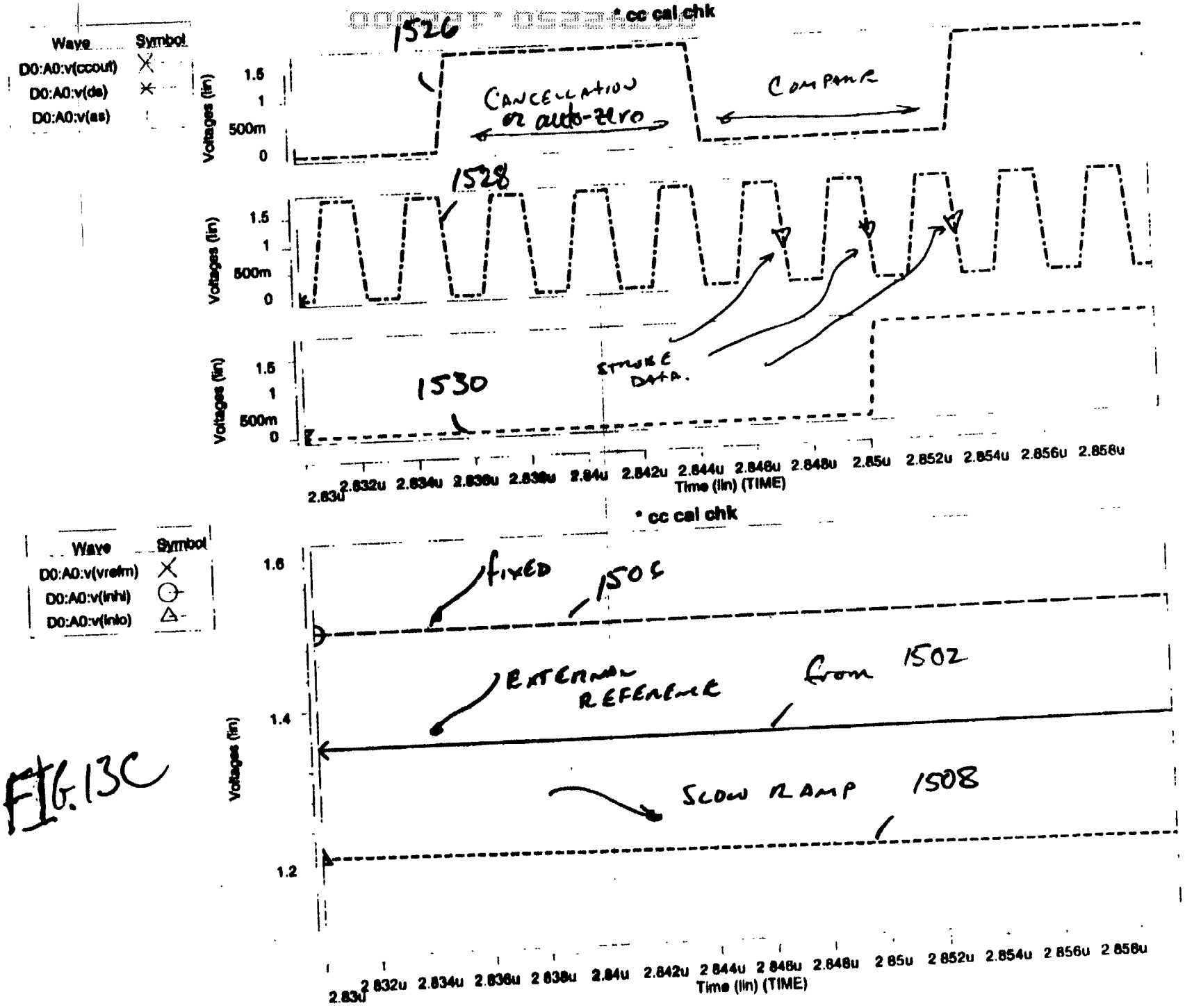
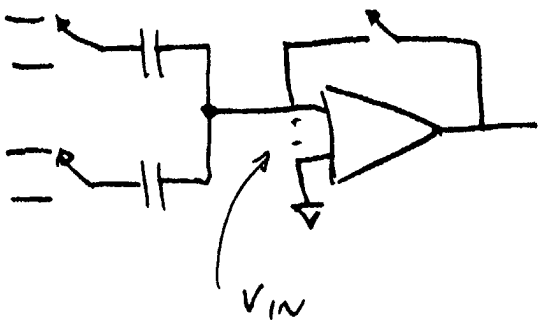

* cc cal chk
Wave
Symbol
D0:A0:v(ccout)
D0:A0:v(ds)
D0:A0:v(as)
Voltages (lin)
1.5
1
500m
0
1526
CANCELLATION
or auto-zero
COMPARE
1528
1530
STROBE
DATA.
2.83u
2.832u
2.834u
2.836u
2.838u
2.84u
2.842u
2.844u
2.846u
2.848u
2.85u
2.852u
2.854u
2.856u
2.858u
Time (lin) (TIME)
* cc cal chk
D0:A0:v(vrefm)
D0:A0:v(inhi)
D0:A0:v(inlo)
1.6
1.4
1.2
FIXED
1506
EXTERNAL REFERENCE
from 1502
SLOW RAMP
1508

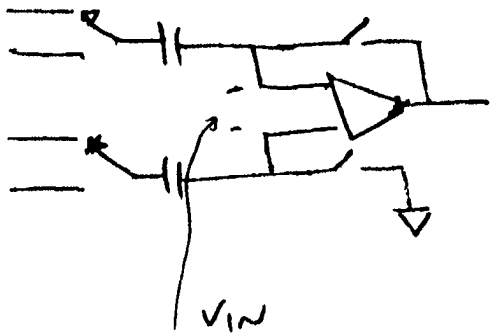
FIG. 13C

Alternate Embodiments of Differential Comparisons

FIG. 13D

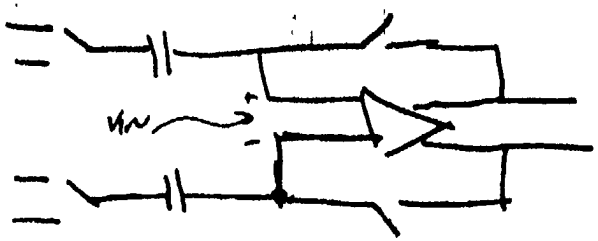


$V_{out} = A \cdot V_{IN}$



$V_{out} = A_v$

DIFFERENTIAL IN SINGLE ENDED OUT



$\pm V_{out} = A \cdot V_{IN}$

Fig. 13E

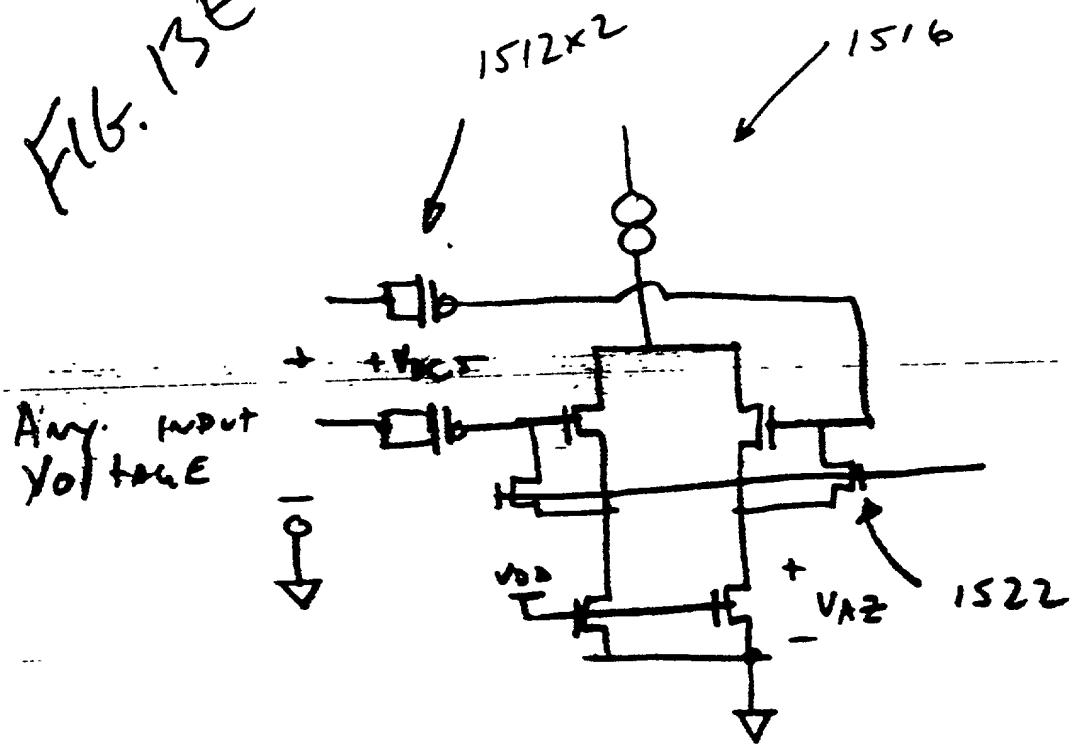


FIG 14A

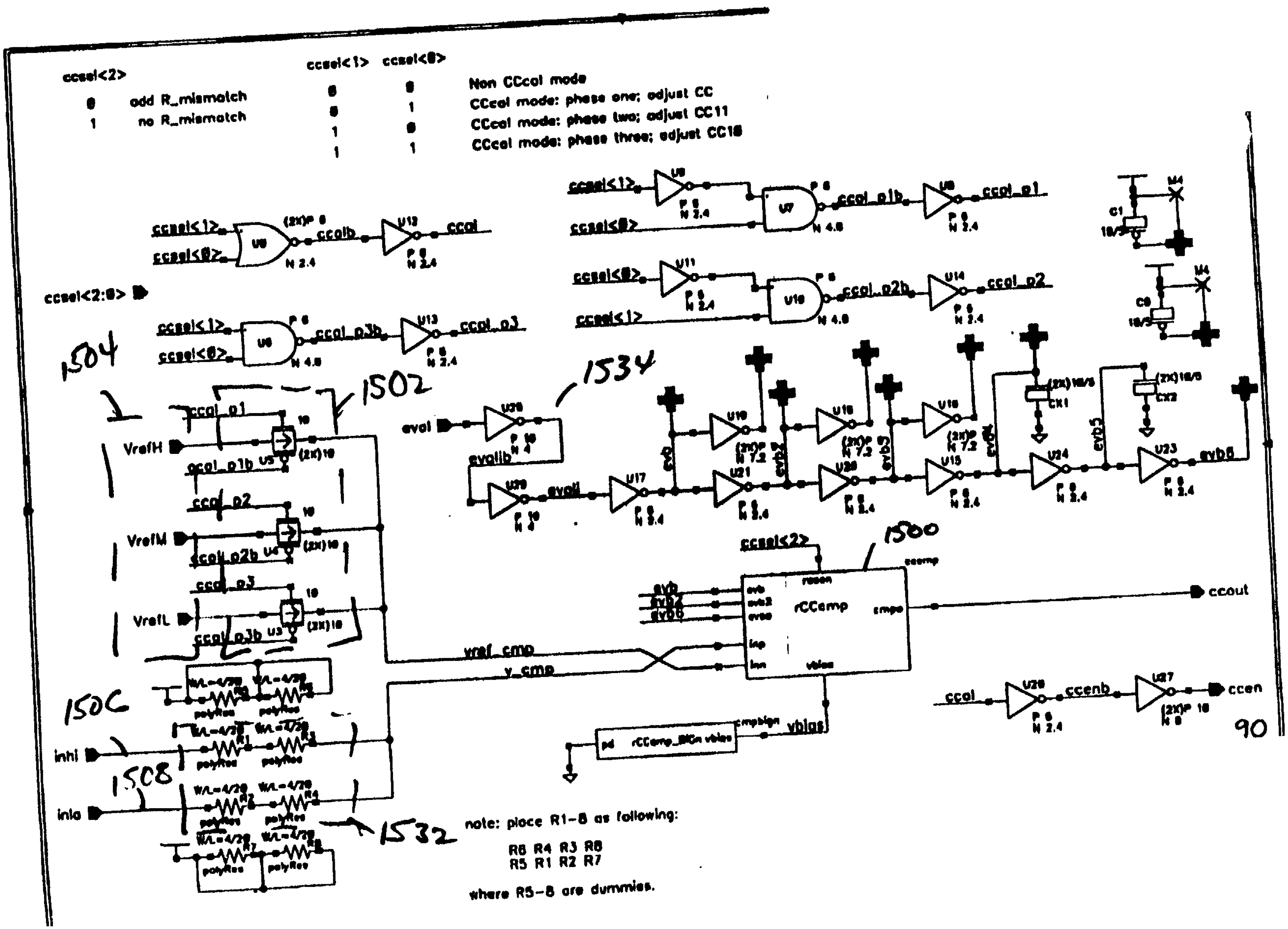

ccsel<2>
0 add R_mismatch
1 no R_mismatch
ccsel<1> ccsel<0>
Non CCcal mode
CCcal mode: phase one; adjust CC
CCcal mode: phase two; adjust CC11
CCcal mode: phase three; adjust CC10
ccsel<2:0>
VrefH
VrefM
VrefL
inhi
inlo
eval
evalib
vref_cmp
v_cmp
rCCcmp
ccout
ccol
ccenb
ccen
vbias
note: place R1-8 as following:
R6 R4 R3 R8
R5 R1 R2 R7
where R5-8 are dummies.
1500
1502
1504
1506
1508
1532
1534
90

FIG 14B

Latching Stage

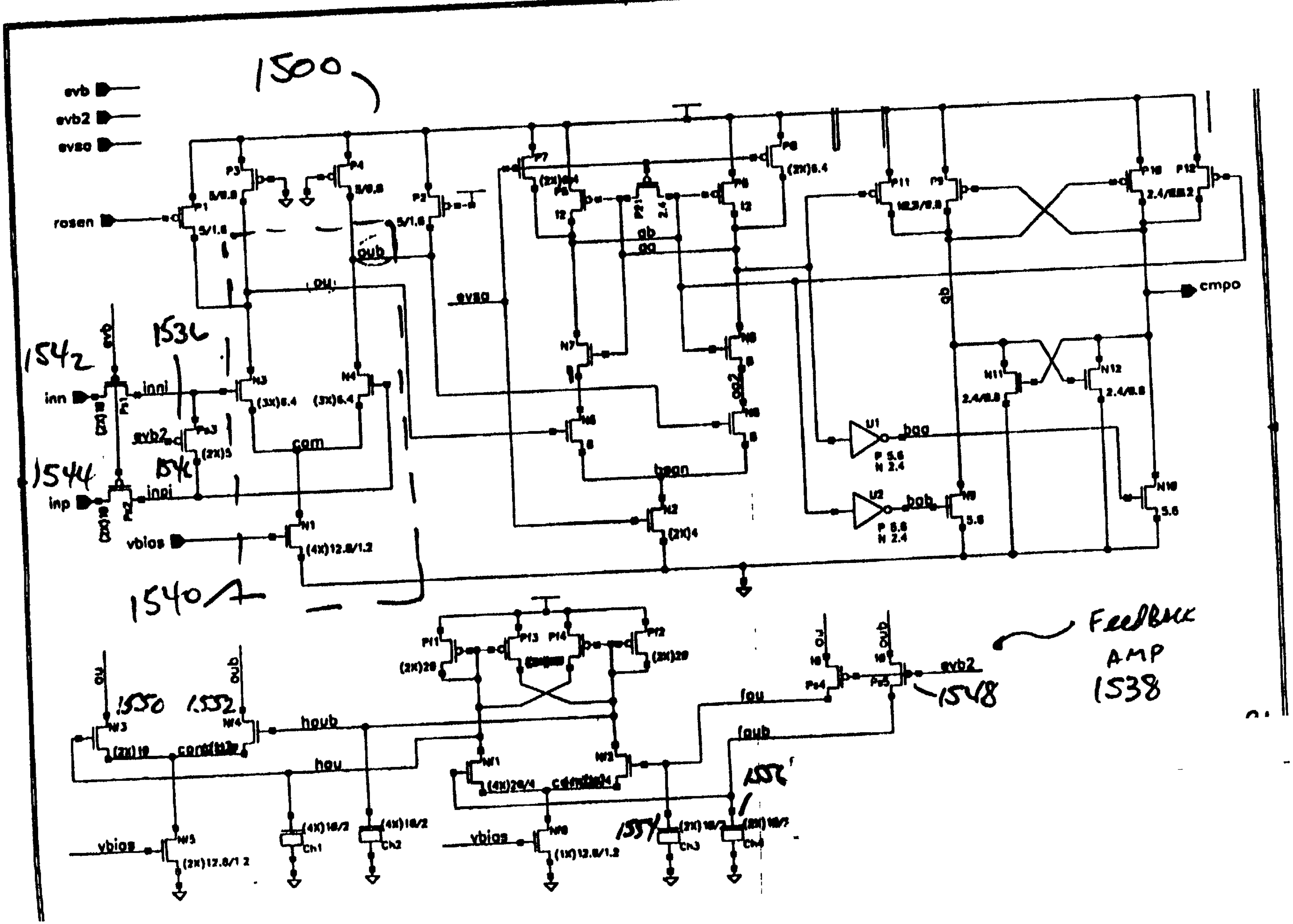


Fig 14C

mismatch w/ os cancellation

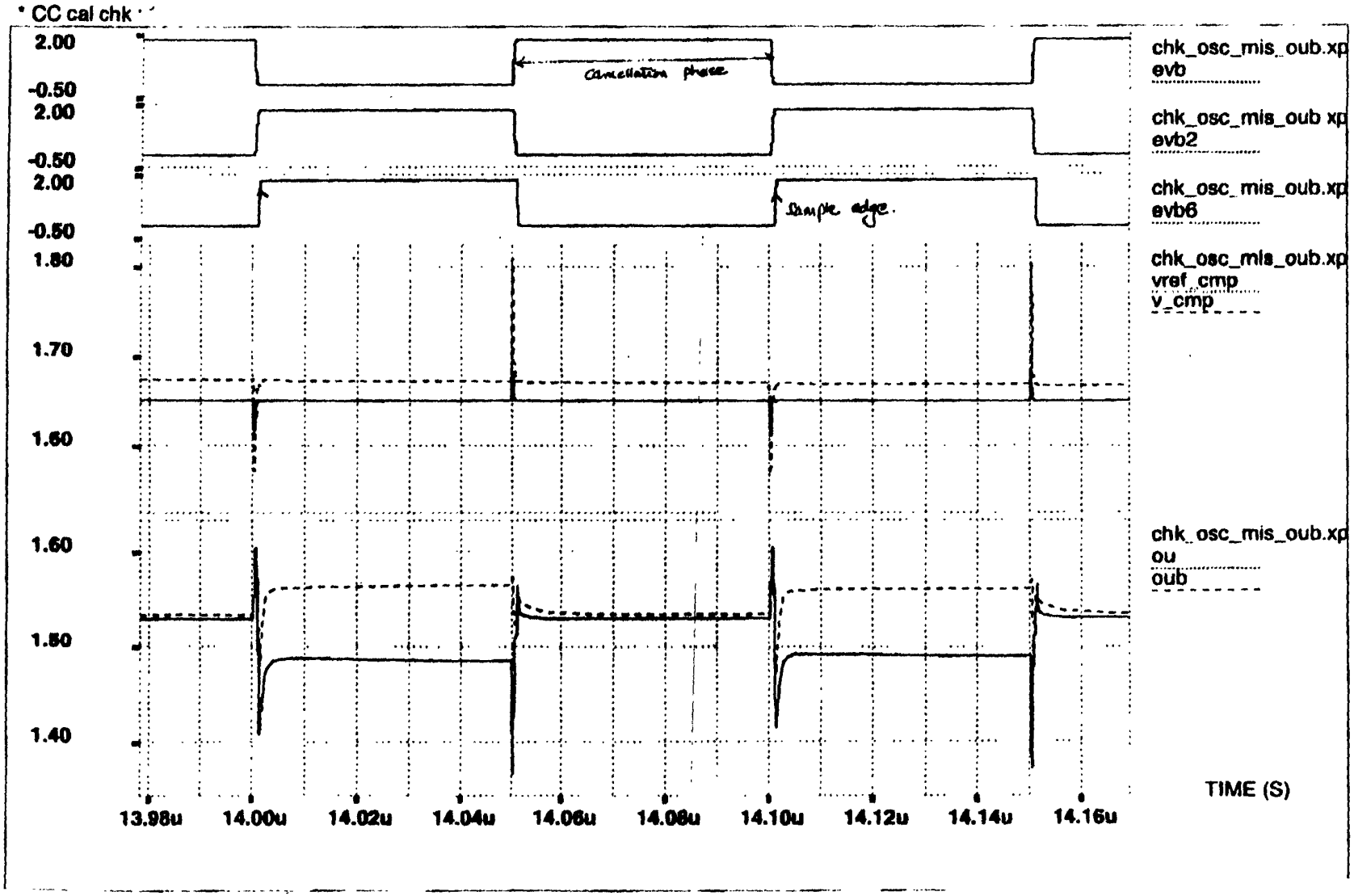


FIG 14D

w/ OS cancel

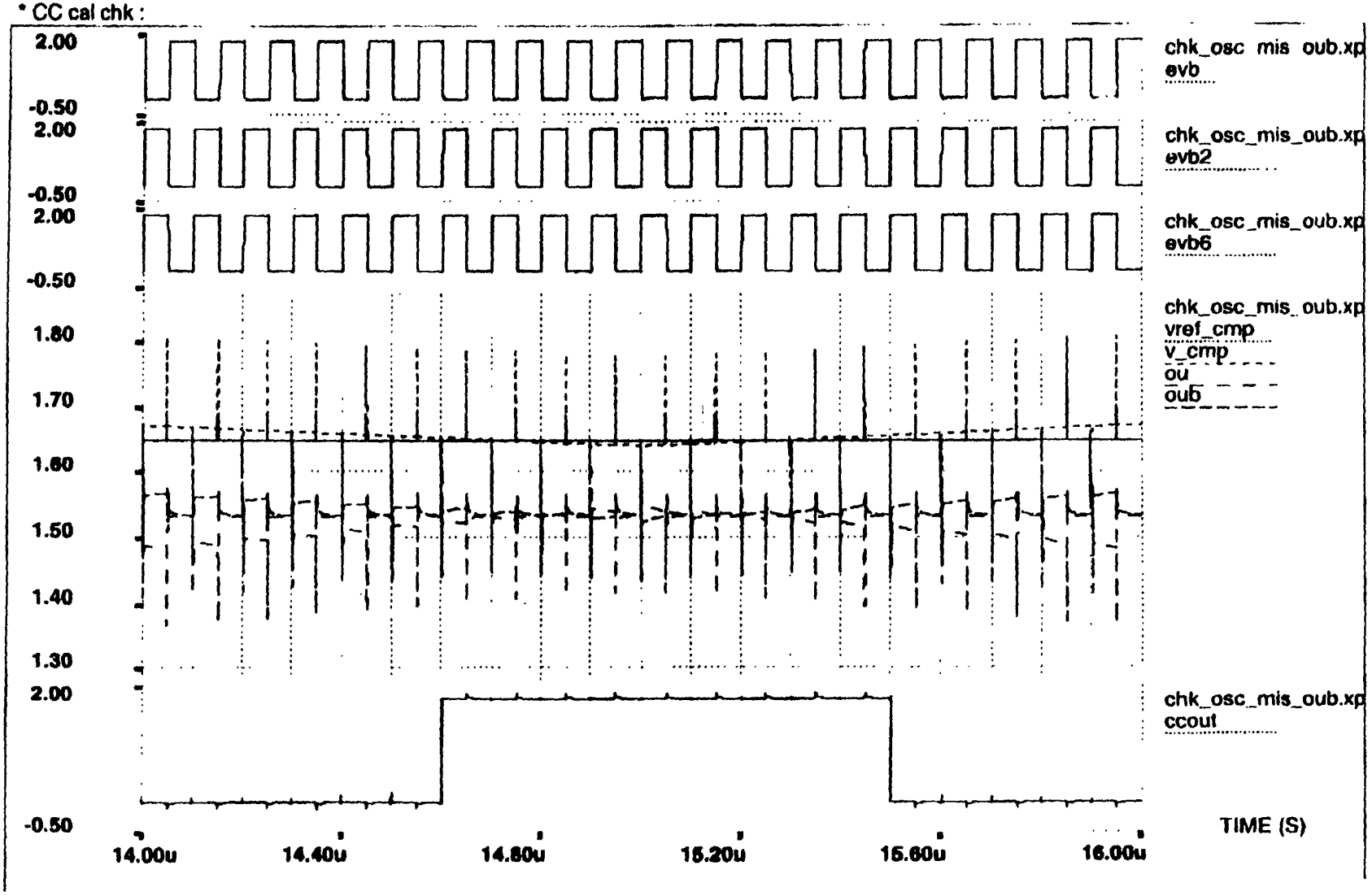
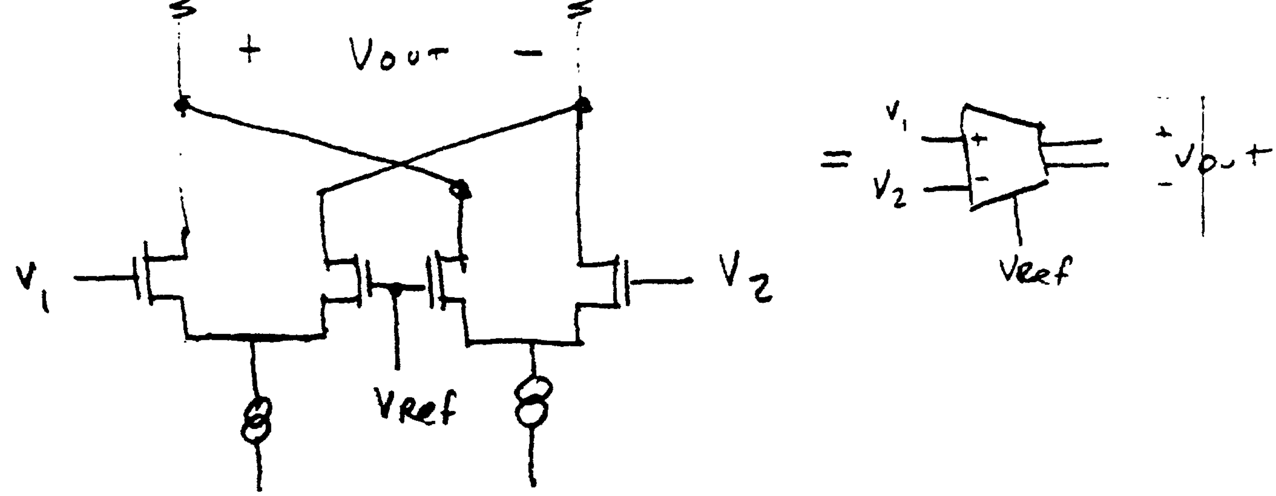


FIG. 15A



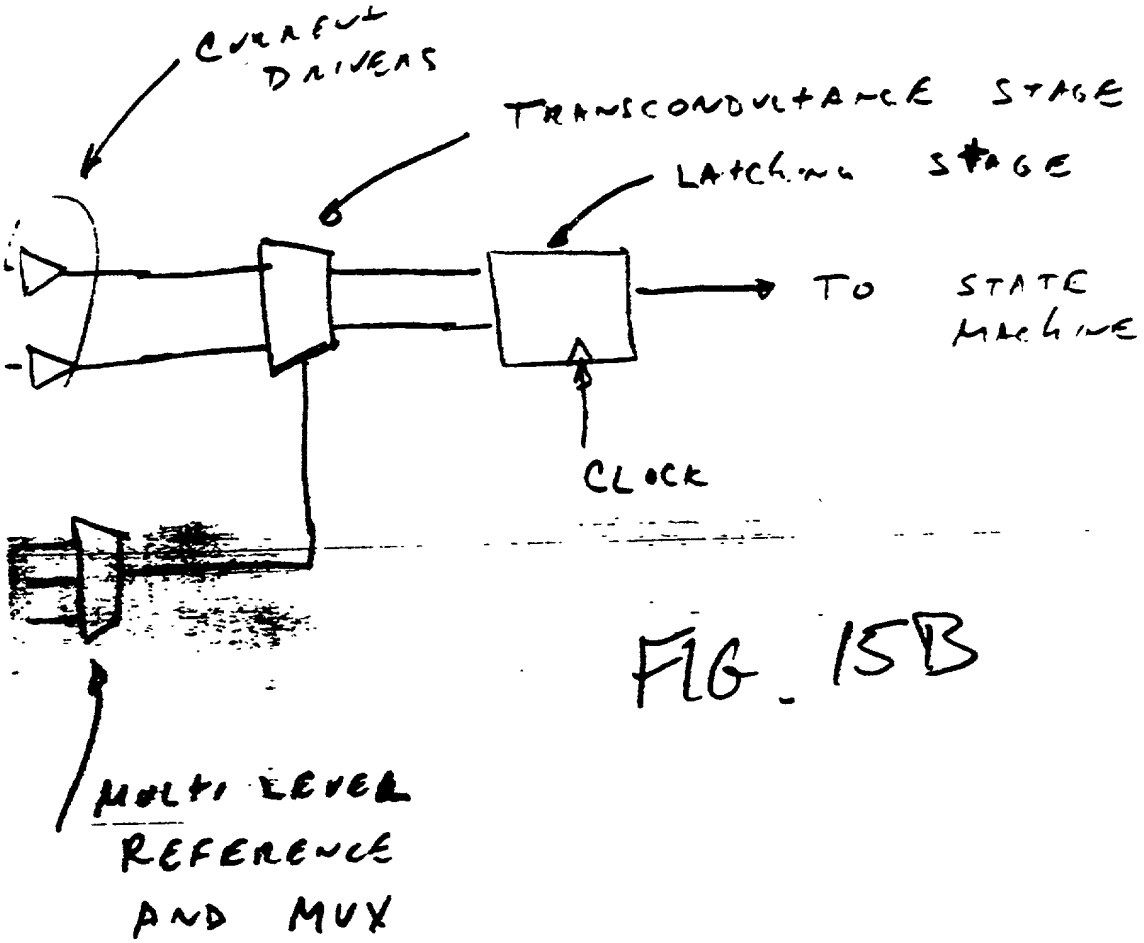


FIG. 15B

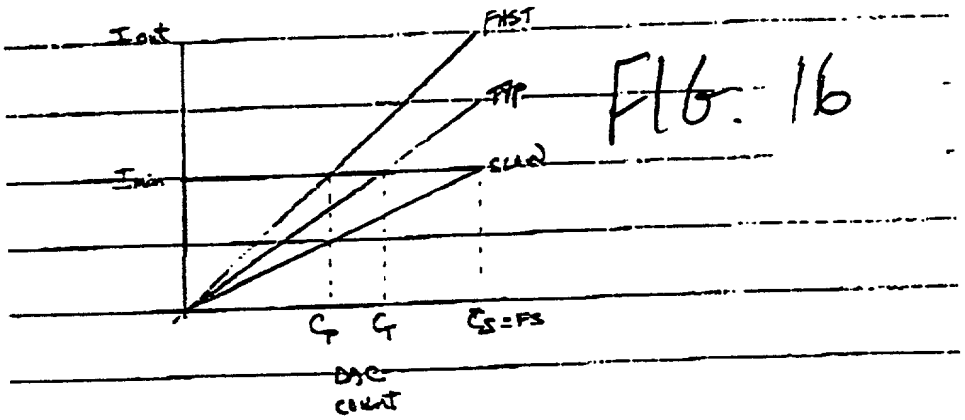


FIG. 16

Output driver block diagram:

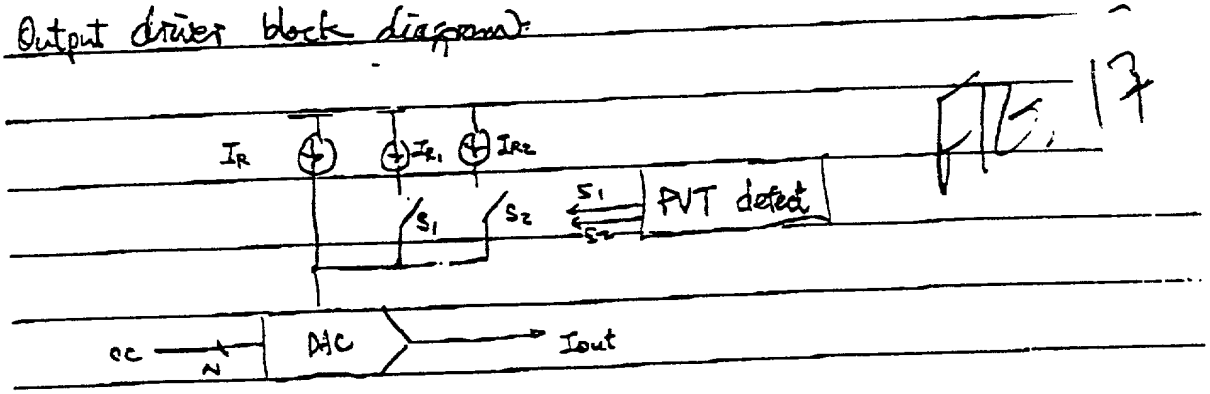
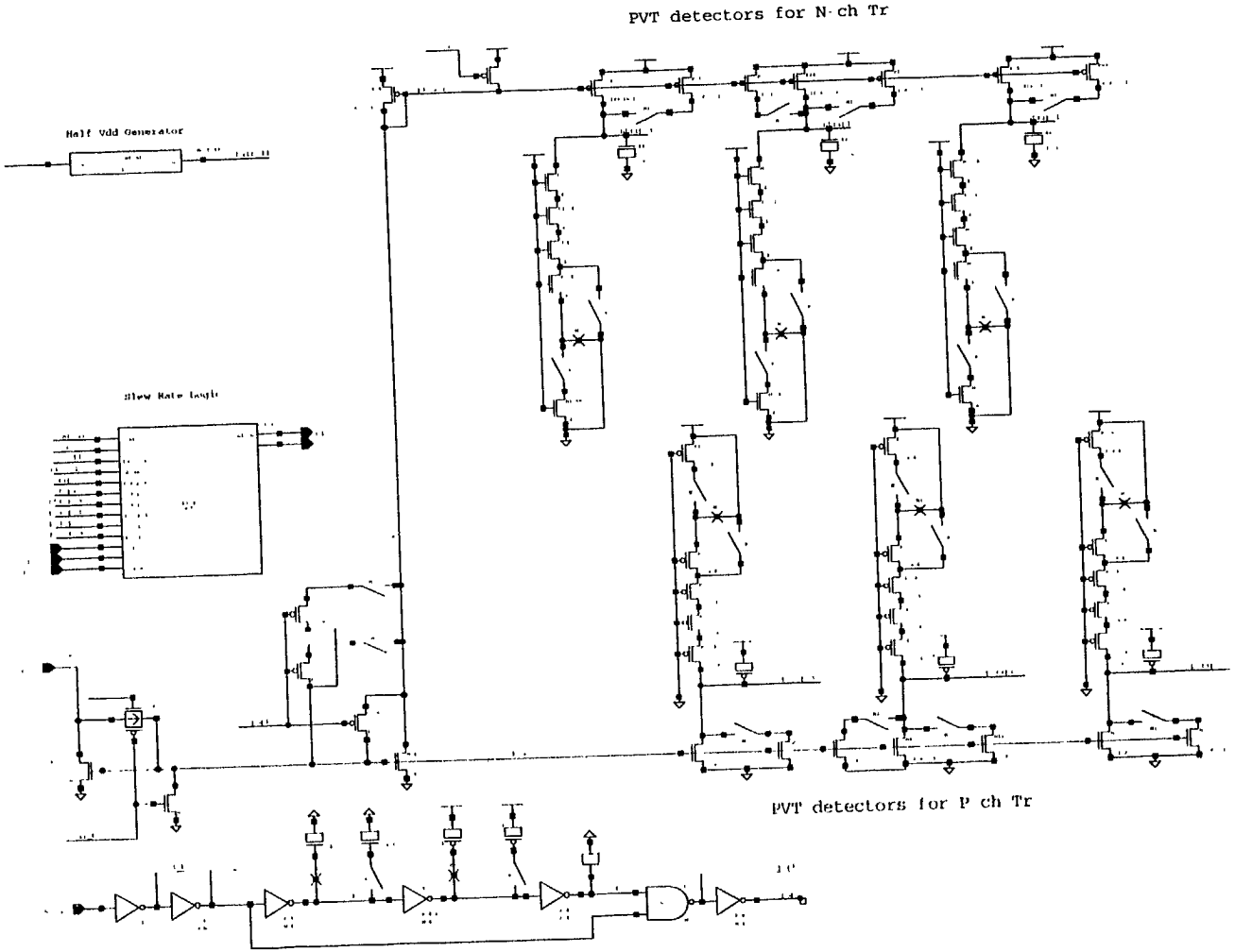


FIG. 17

FIG. 18


PVT detectors for N-ch Tr
Half Vdd Generator
Slew Rate Logic
PVT detectors for P ch Tr

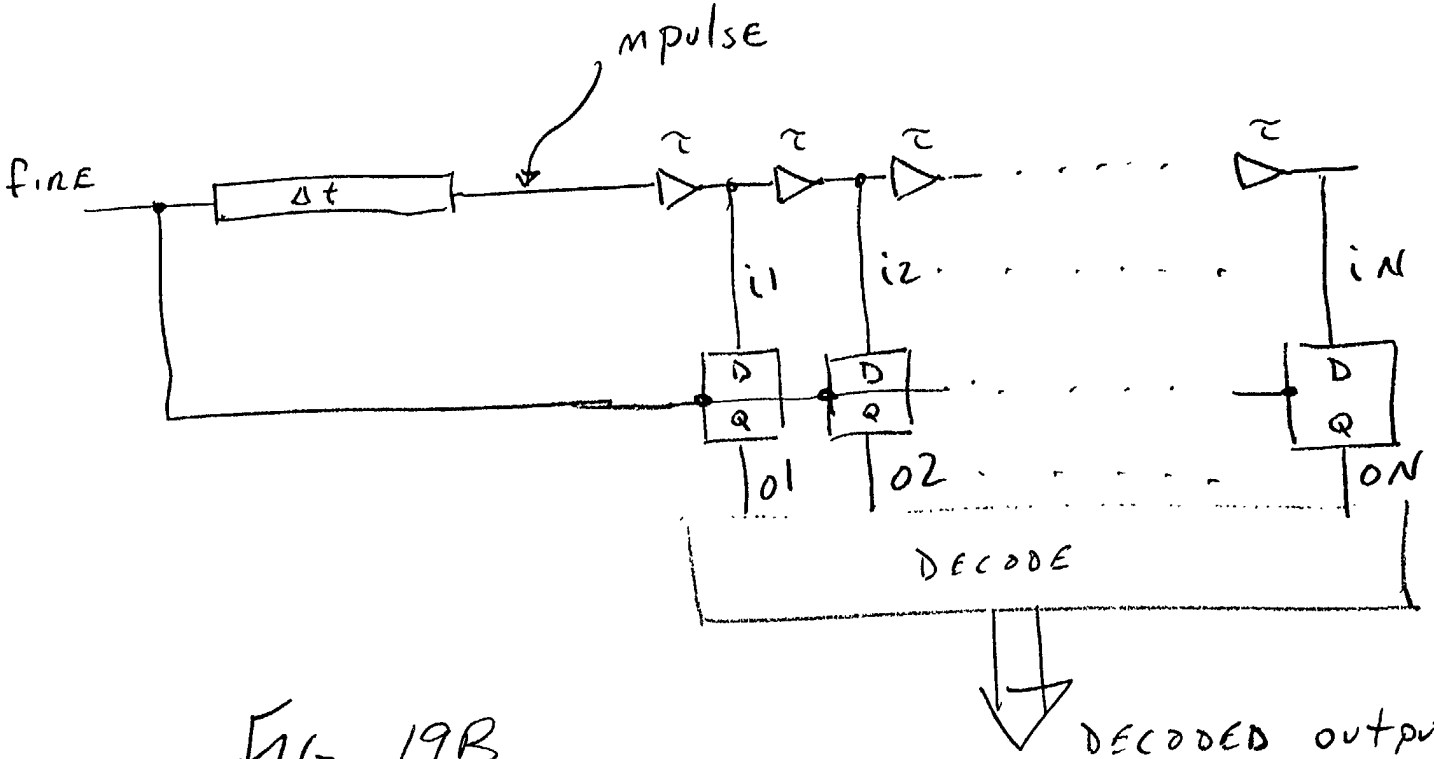


FIG. 19A

FIG. 19B

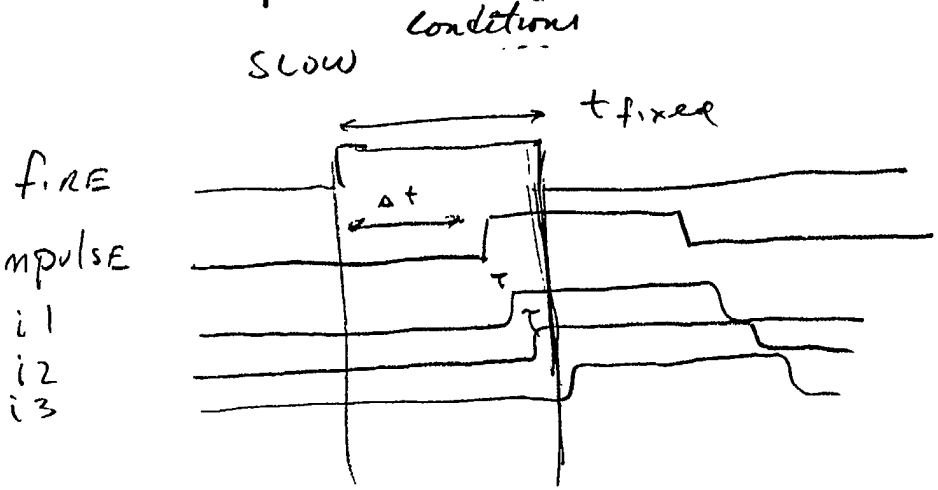


FIG 19C

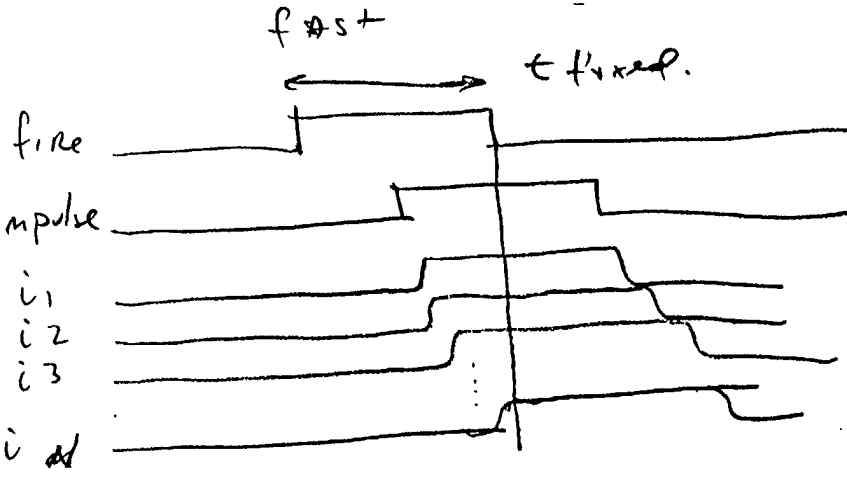
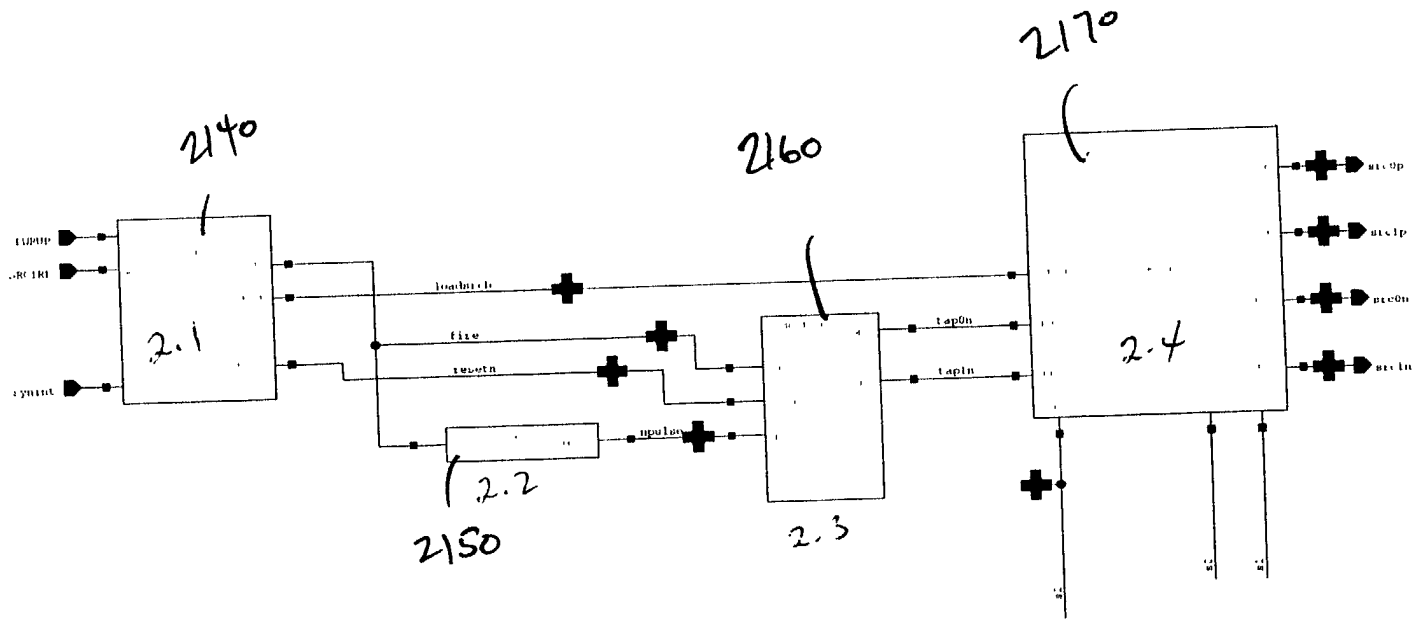
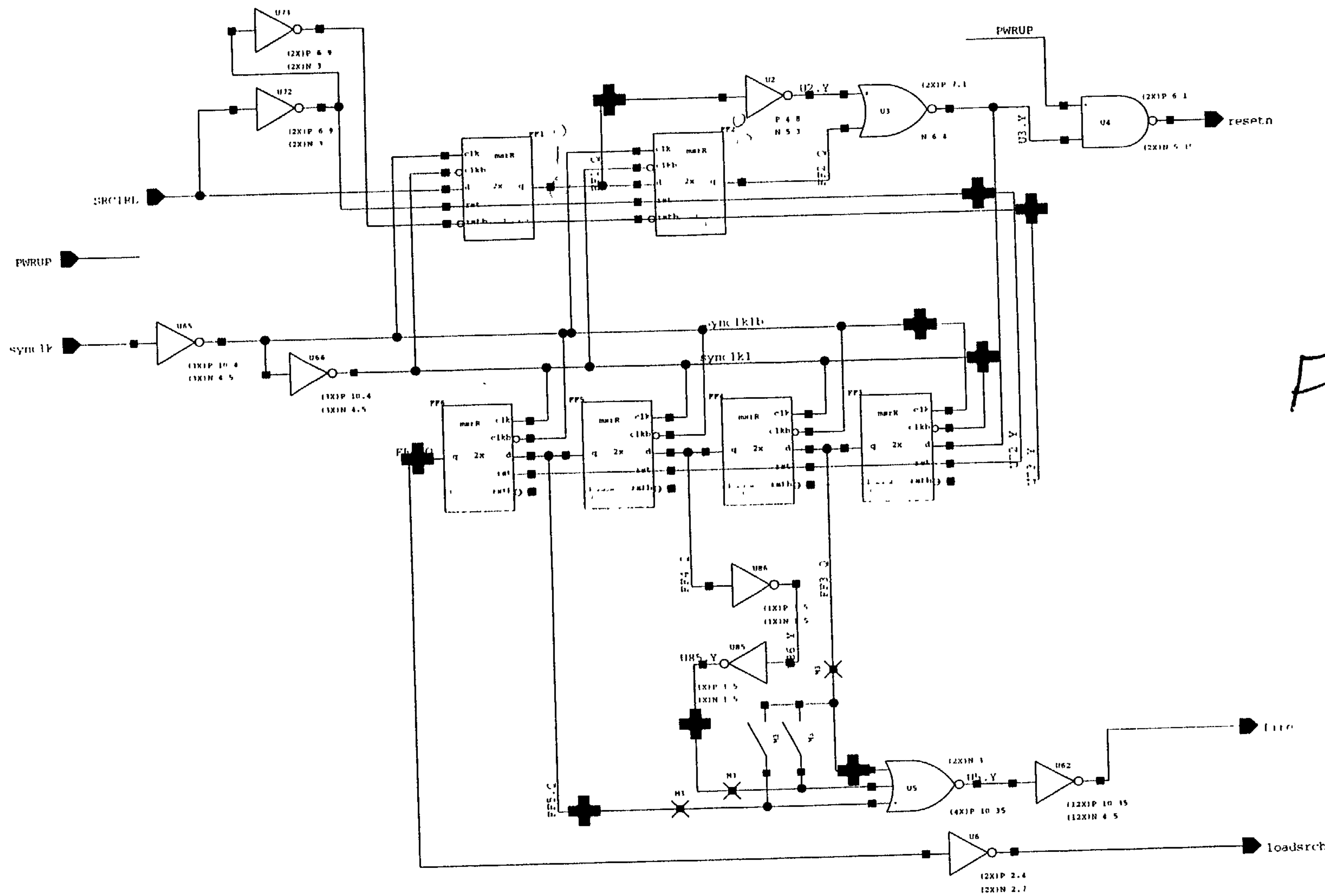


FIG 20A





PWRUP
resetn
SRCTRL
PWRUP
synclk
synclklb
synclkl
U2
U2.Y
U3
U3.Y
U4
U5
U6
U62
U64
U65
U71
U72
U85
U86
fire
loadsrch

FIG 20B

FIG 20C

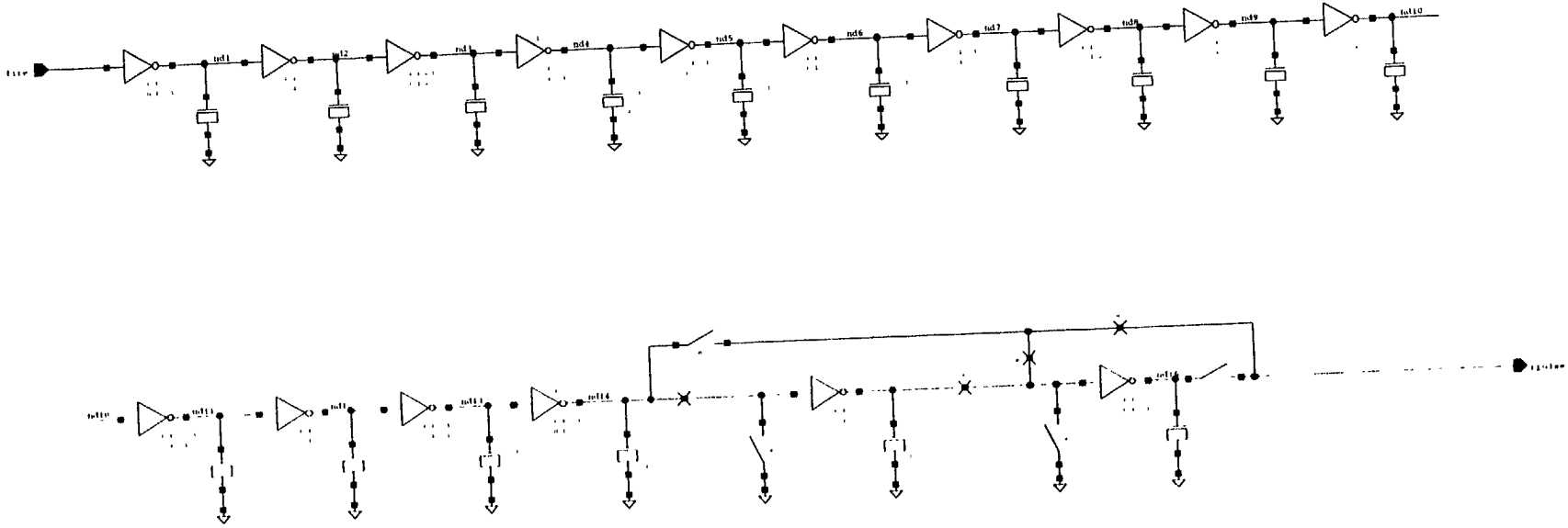
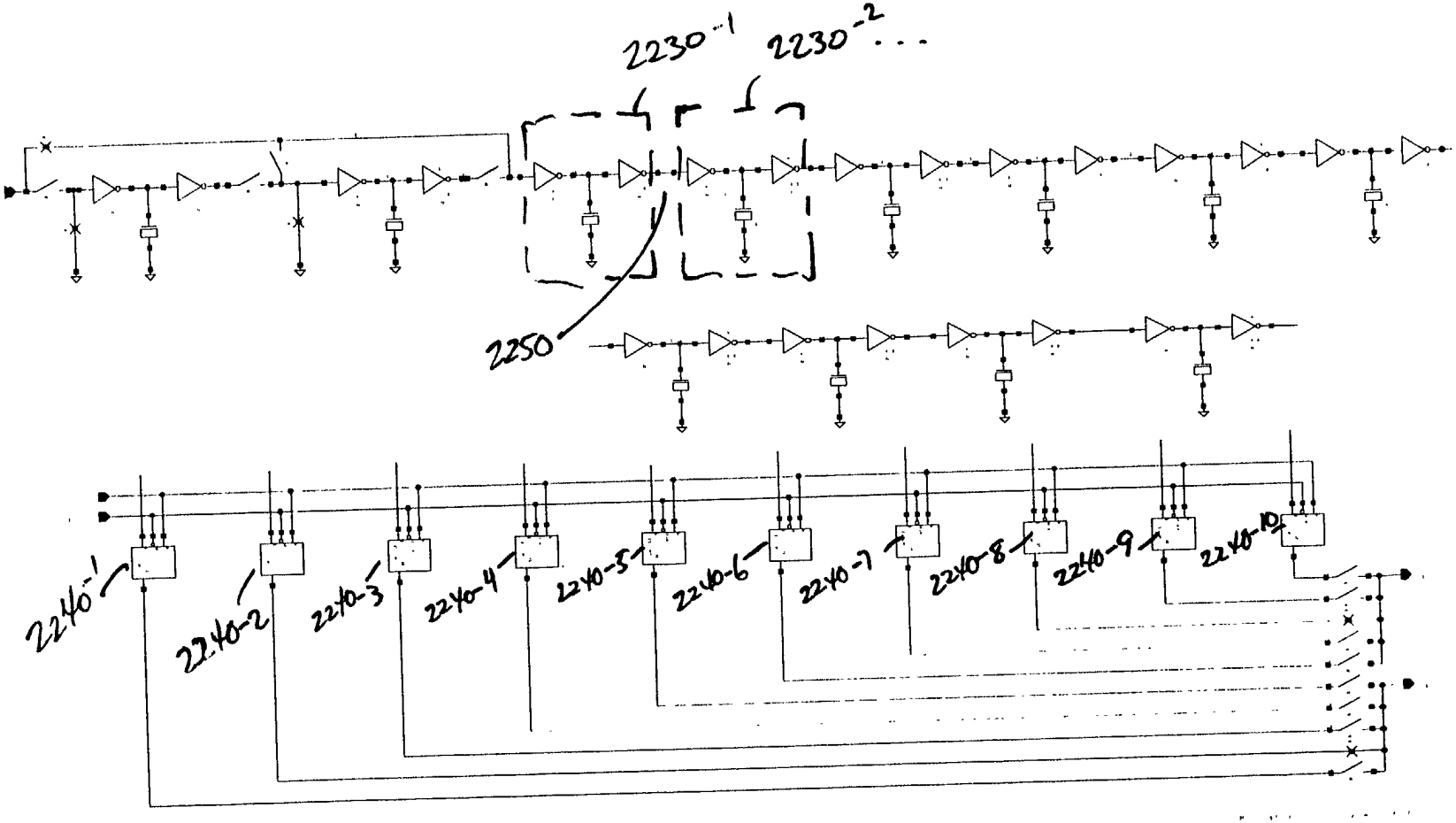


Fig. 20D


2230-1
2230-2
2250
2240-1
2240-2
2240-3
2240-4
2240-5
2240-6
2240-7
2240-8
2240-9
2240-10

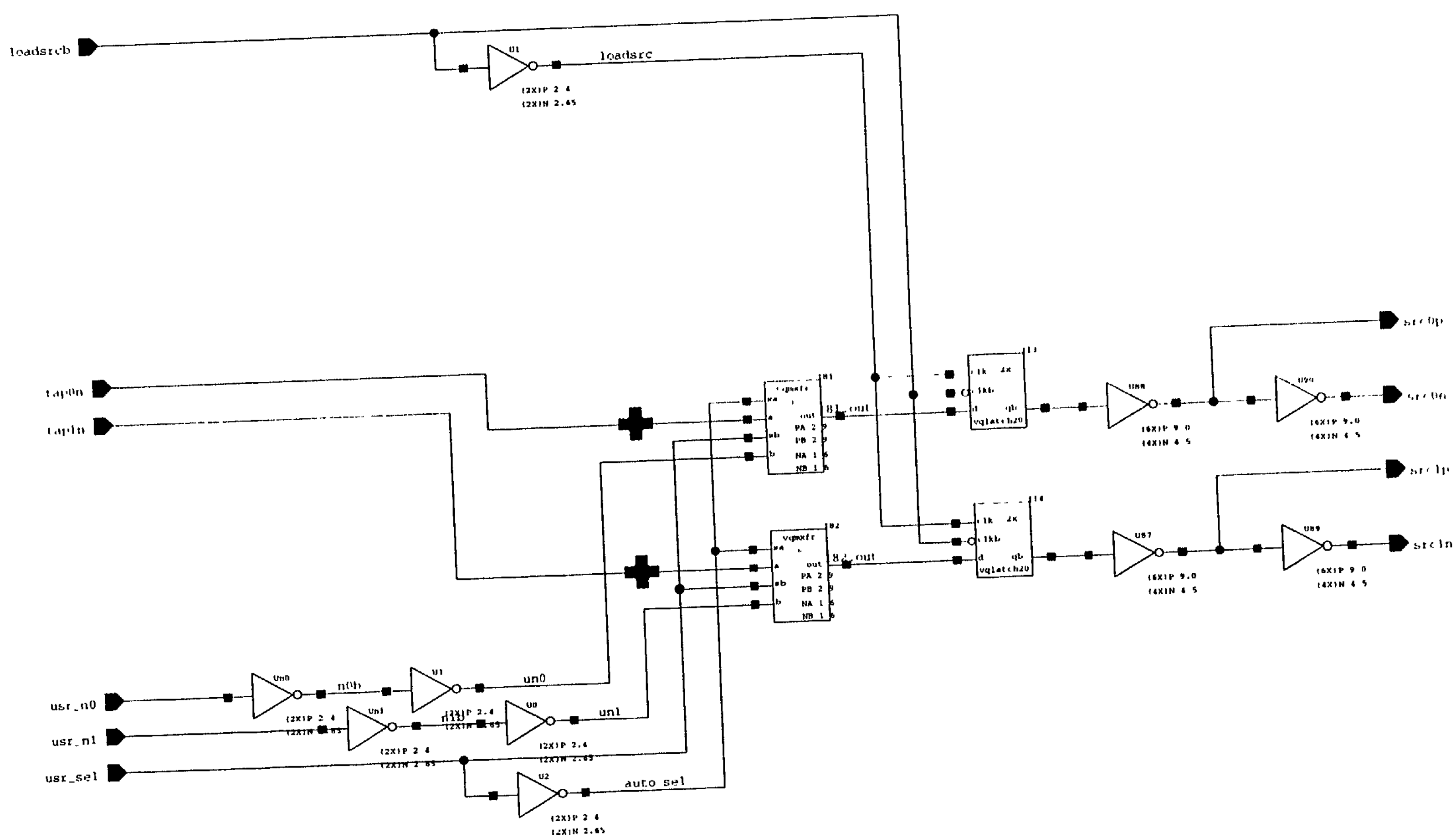

loadsrcb
U1
(2X)P 2 4
(2X)N 2.65
loadsrc
tap0n
tap1n
usr_n0
usr_n1
usr_sel
Un0
n0b
U1
un0
Un1
n1b
U0
un1
U2
auto sel
B1_out
B2_out
out
PA 2
PB 2
NA 1
NB 1
vqlatch20
clk
qb
d
U88
U90
U87
U89
(6X)P 9.0
(4X)N 4 5
src0p
src0n
src1p
src1n

FIG 20E

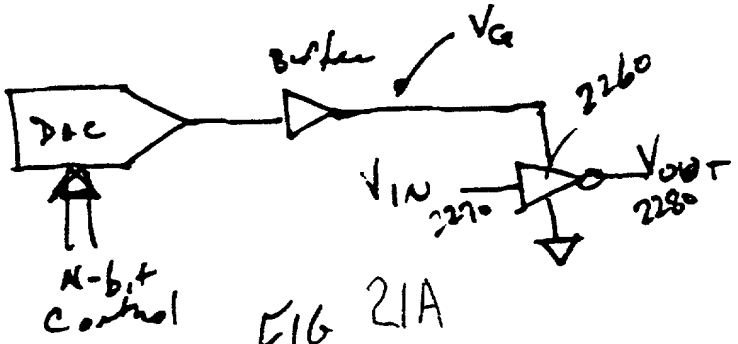


FIG 21A

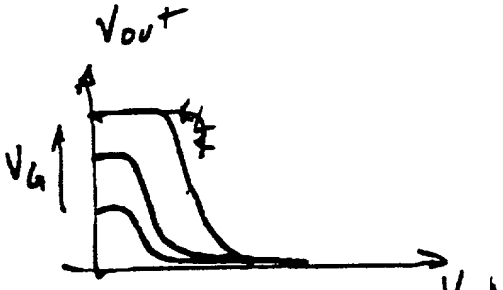


FIG 21B

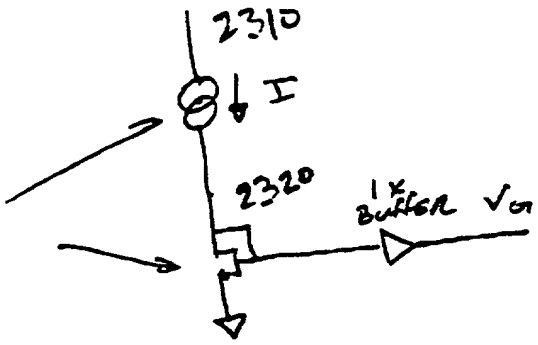


FIG 22

ALTERNATE EMBODIMENT of V_{GATE} DAC

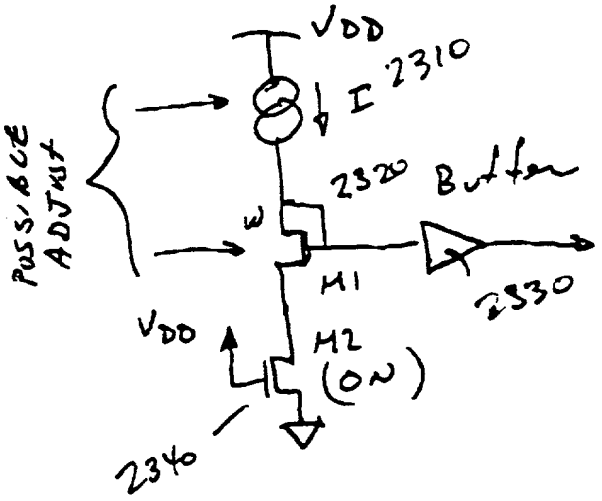


Fig. 23

M1, M2 SCALED to MATCH Actual output DRIVER.

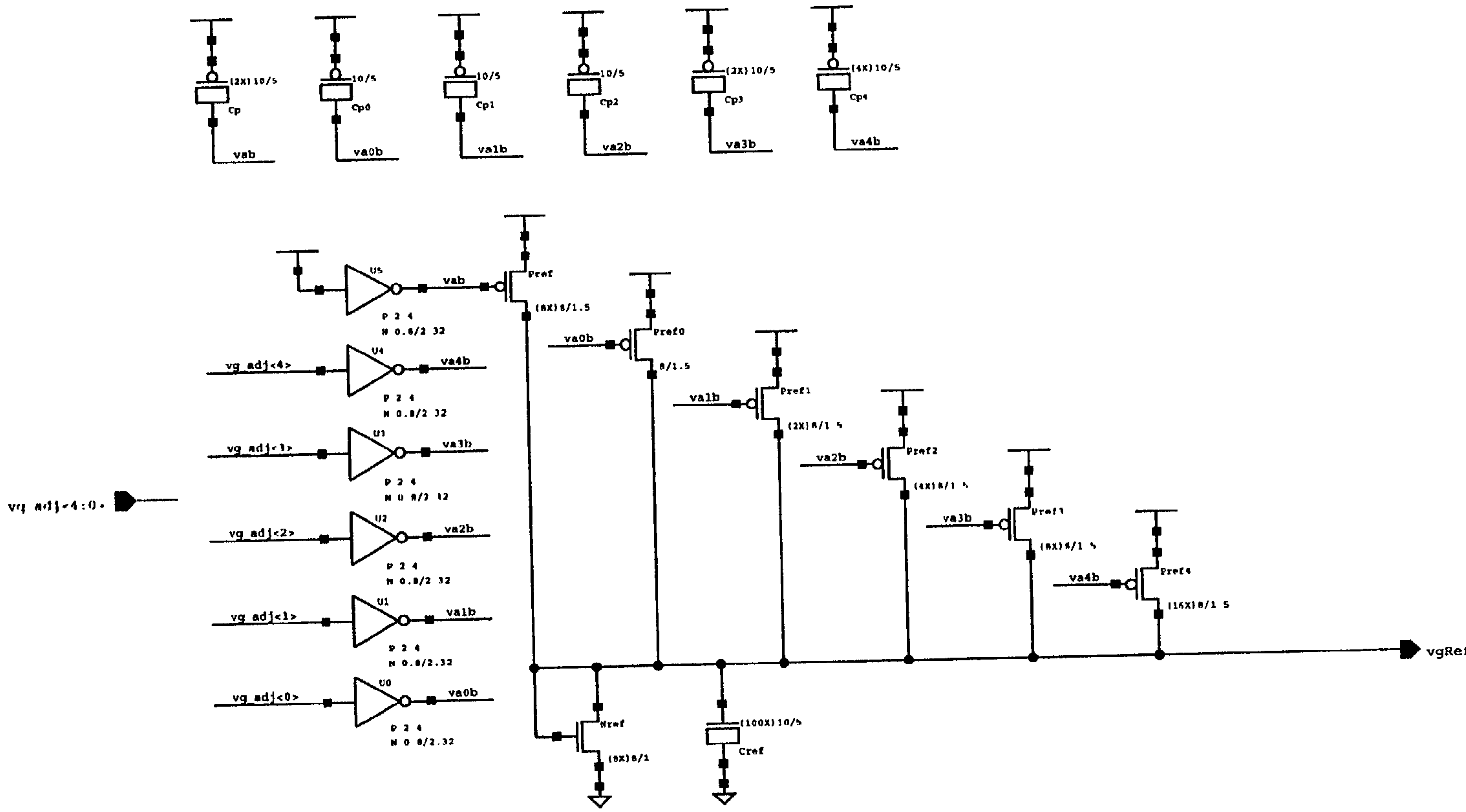

(2X)10/5
Cp
vab
10/5
Cp0
va0b
10/5
Cp1
va1b
10/5
Cp2
va2b
(2X)10/5
Cp3
va3b
(4X)10/5
Cp4
va4b
U5
vab
P 2 4
N 0.8/2 32
Pref
(8X)8/1.5
U4
vg_adj<4>
va4b
P 2 4
N 0.8/2 32
U3
vg_adj<3>
va3b
U2
vg_adj<2>
va2b
P 2 4
N 0.8/2 32
U1
vg_adj<1>
va1b
P 2 4
N 0.8/2.32
U0
vg_adj<0>
va0b
P 2 4
vg_adj<4:0>
va0b
Pref0
8/1.5
va1b
Pref1
va2b
Pref2
va3b
va4b
Pref4
Nref
(8X)8/1
(100X)10/5
Cref
vgRef

FIG. 24A

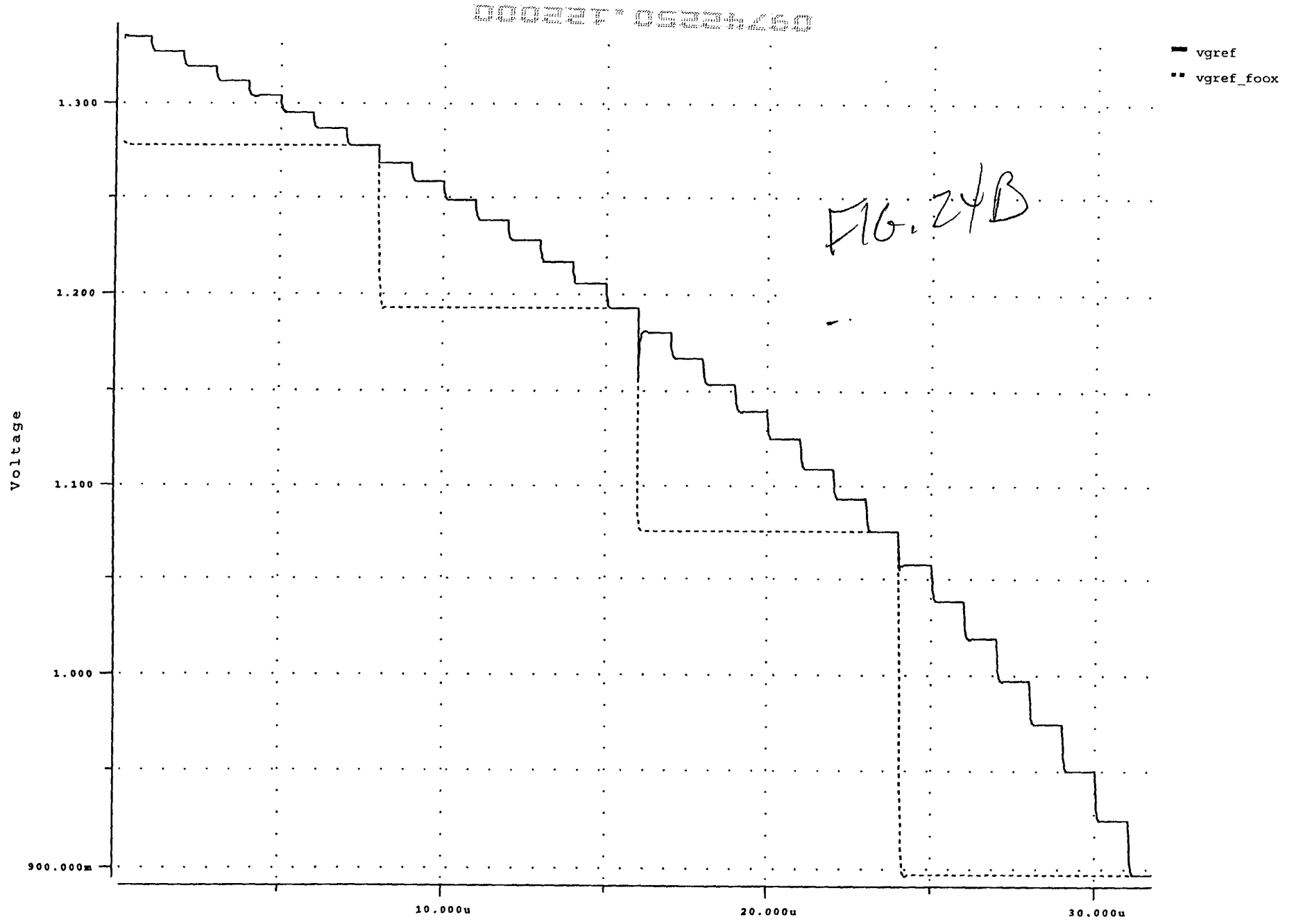

vgref
vgref_foox
1.300
1.200
1.100
1.000
900.000m
Voltage
10.000u
20.000u
30.000u

FIG. 24B